Transverse Feedback System (LHC Damper)

Outline of Presentation

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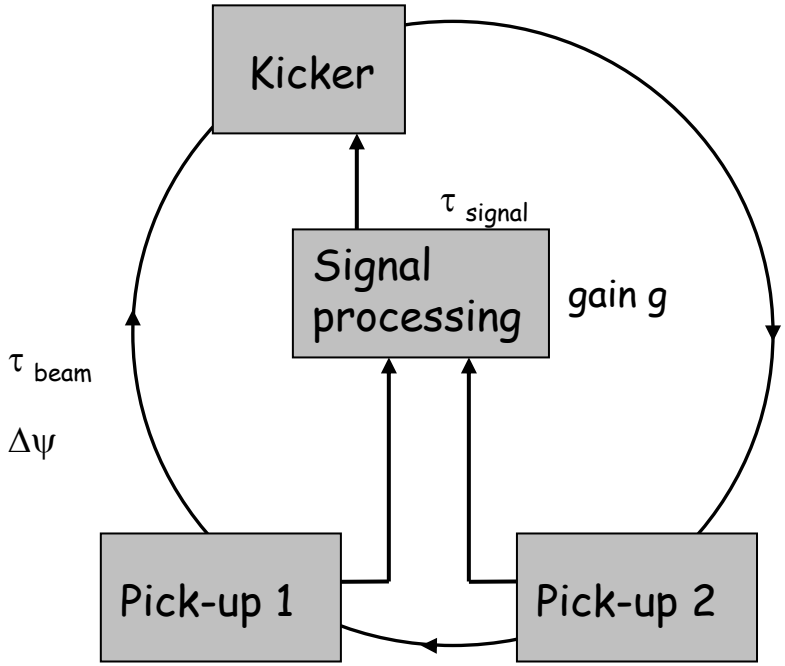
- Overview: Transverse feedback systems (dampers) at CERN's synchrotrons (PS Booster, AD, LEIR, PS, SPS and LHC); example: SPS damper
- Functional Specification and overview of LHC Damper System
- Collaboration with JINR, Dubna for feedback kickers and tetrode power amplifiers
- Test area, interlocks and industrial controls
- 200 W driver amplifiers (TCB Thales Belgium)
- Plans for the low-level signal processing and synergy with related projects for LHC and PS (longitudinal 1-Turn cavity feedbacks)

Transverse multi bunch feedback



Need real-time digital signal processing

Match delays:

$\tau_{signal} = \tau_{beam} + MT_0$

T0 : beam revolution time

M=1: very common -> "One -Turn-Delay" feedback

Need means for phase *and* delay adjustments

- damping: of transverse injection oscillations
- feedback: curing transverse coupled bunch instabilities
- excitation: of transverse oscillations for beam measurements & other applications

Transverse Feedback Systems in Synchrotrons at CERN

Currently *installed* transverse feedback systems in CERN Synchrotrons

Accelerator	Digital / analogue processing	Power / kicker / bandwidth	Usage in operation
PS Booster (protons) 50 MeV – 1.4 GeV kin. E.	multi turn injection from linac analogue beam offset signal suppression, analogue delay (cables & switches)	100 W, 50 Ω stripline Limited to 30 MHz in operation But built for 100 MHz bandwidth baseband	H-plane: **used and required** V-plane: beam stable w/o FB
AD (anti-proton decelerator) 3.57 GeV – 0.1 GeV	Copy of booster system	100 W, 50 Ω stripline 100 MHz bandwidth baseband	used only for excitation purposes
SPS (protons, ions) (14 – 450) GeV/c protons FT (26 – 450) GeV/c LHC beam	digital notch filter and 1T-delay (Altera FPGA, 80 MHz clock) commissioned in 2000/2001	tetrode amplifiers with two 30 kW tetrodes in push-pull directly coupled to a kicker (base band); feedback bandwidth ~10 kHz to 20 MHz	H-plane: used in operation V-plane: used in operation **used and required for operation** above $5x10^{12}$ protons (max ~$5.5x10^{13}$ ppp accelerated)

Transverse Feedback Systems in Synchrotrons at CERN

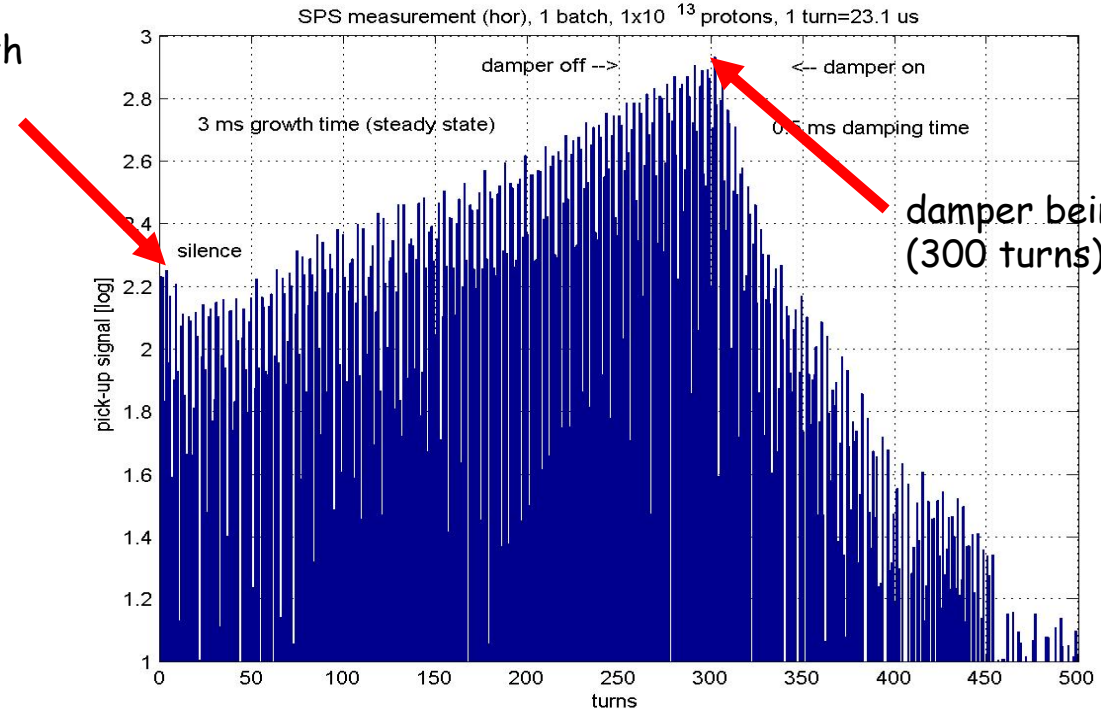
Current transverse feedback system *projects* at CERN

Accelerator	Digital / analogue processing	Power / kicker / bandwidth	Planned commissioning and usage
LEIR (ions: Pb^{54+}) 4.2 MeV/u – 72 MeV/u	copy of PS Booster System	100 W, 50 Ω stripline	**2005** damping during e-cooling may be necessary
PS (protons, ions) 1.4 GeV – 25 GeV (kinetic E)	synergy with LHC Damper	3 kW pulsed, 200 W CW, 50 Ω stripline with ~30 MHz bandwidth in baseband, lower cut-off ~50 kHz ? upgrade possible with magnetic kicker (0.9 m length, 12.5 W, but bandwidth considered too limited); H-plane magnetic kicker built already	**2006** injection damping and feedback will be beneficial in particular for high intensity CNGS beams and LHC beams. Currently horizontal instabilities are cured by introducing coupling to the vertical plane which constrains the tunes
LHC (protons, ions) pProtons: 450 GeV/c – 7 TeV/c	digital notch filter and 1T-delay, built-in diagnostics 14 bit ADC/DAC Altera FPGA, 80 MHz clock new development in progress	tetrode amplifiers with two 30 kW tetrodes in push-pull directly coupled to kicker (base band) similar to SPS system 3 kHz -> 20 MHz	**2007** injection damping feedback loop clsoed during ramp switch off during physics?

Example SPS (CNGS type beam, 1 batch, 10^{13} protons):

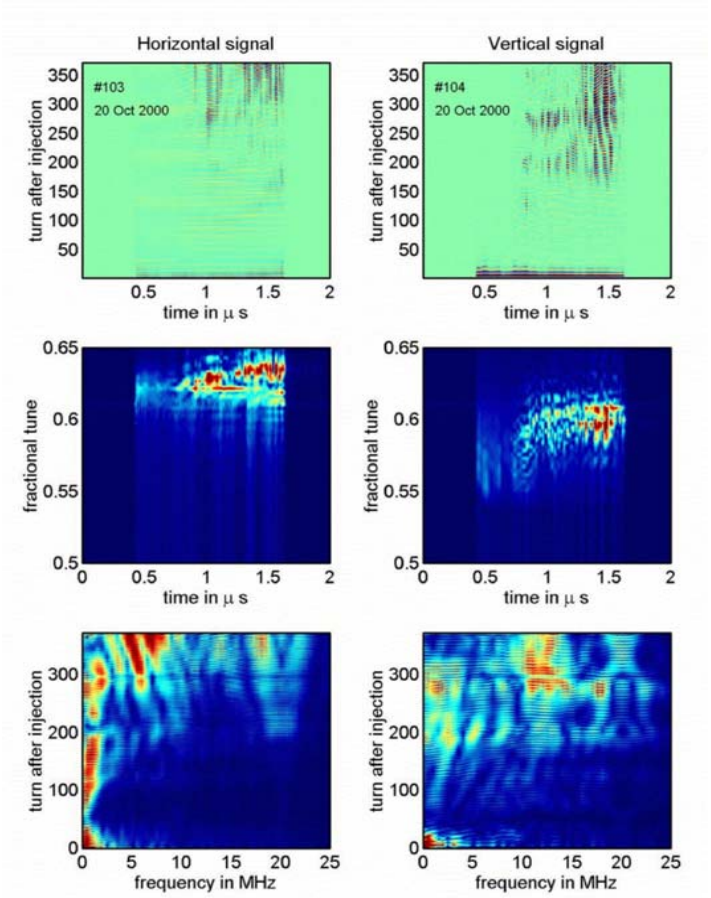
3 ms growth rate
0.5 ms damping time

injection with damper off

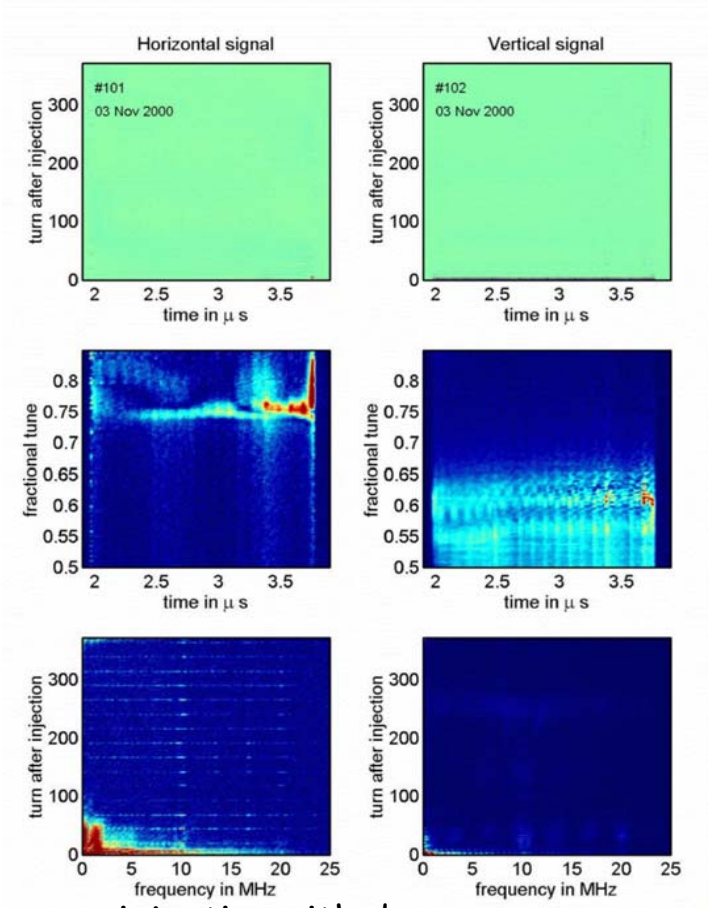


damper being switched on 7 ms (300 turns) after injection

Example SPS (LHC beam, 48 / 72 bunches spaced 25 ns)

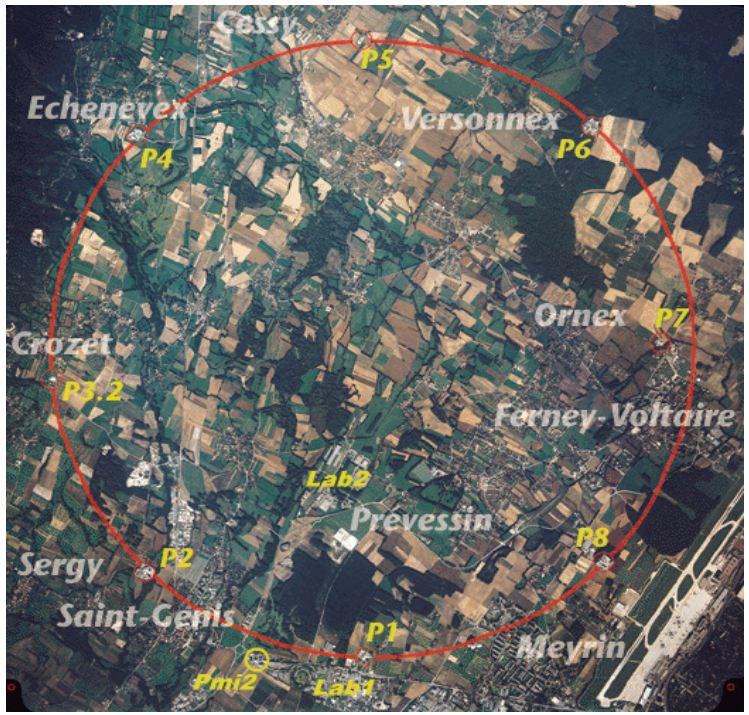


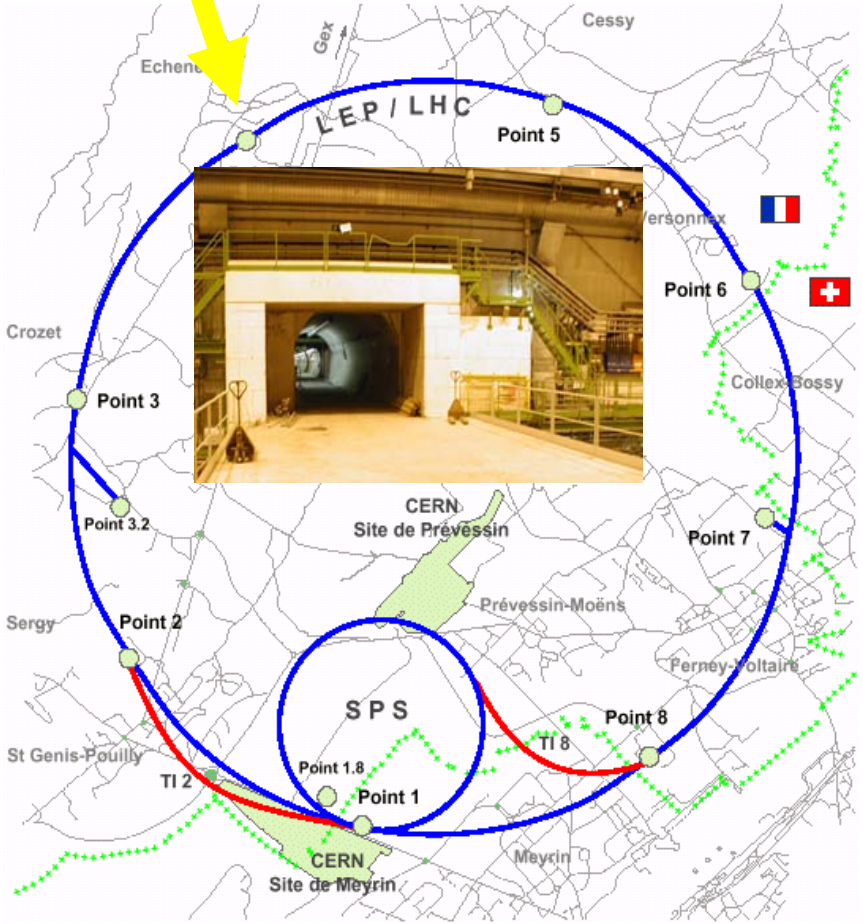
injection with damper off
(~4x10[12] p total in 48 bunches)



injection with damper on
(~6x1012 p total in 72 bunches)

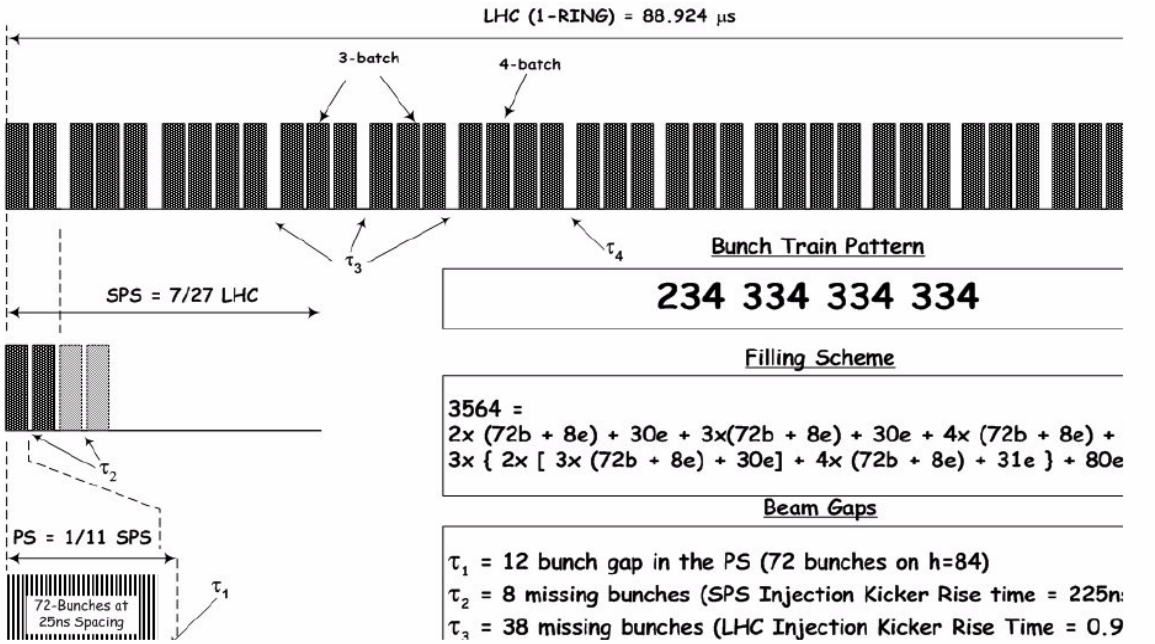
LHC Damper will be installed in point 4 of LHC along with the accelerating 400 MHz RF system





Nominal LHC filling pattern: 2808 bunches

- Basic bunch spacing is 25 ns (every 10th bucket of 400 MHz RF)
- Running-in with 75 ns bunch spacing possible
- Trains of 72 bunches created in PS accelerator
- Up to 4x72 bunches accelerated in SPS and injected into LHC
- 1 μs gap between batches injected into LHC



Performance specification (1)
(LHC Design Report)

Beam parameters and requirements for nominal intensity:

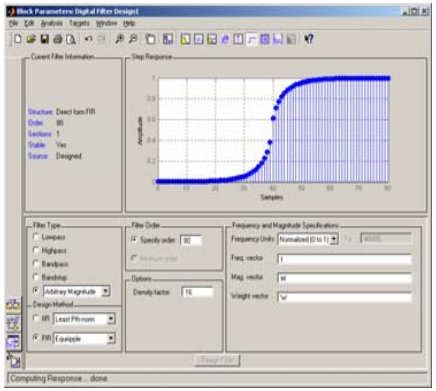
Injection beam momentum	450 GeV/c
Static injection errors	2 mm (at β_{max}=183 m)
ripple (up to 1 MHz)	2 mm (at β_{max}=183 m)
resistive wall growth time	18.5 ms
assumed de-coherence time	68 ms
tolerable emittance growth	2.5 %
Overall damping time	4.1 ms (46 turns)
bunch spacing	25 ns
minimum gap between batches	995 ns
lowest betatron frequency	> 2 kHz
highest frequency to damp	20 MHz

Performance specification (2)

Equipment performance specification:

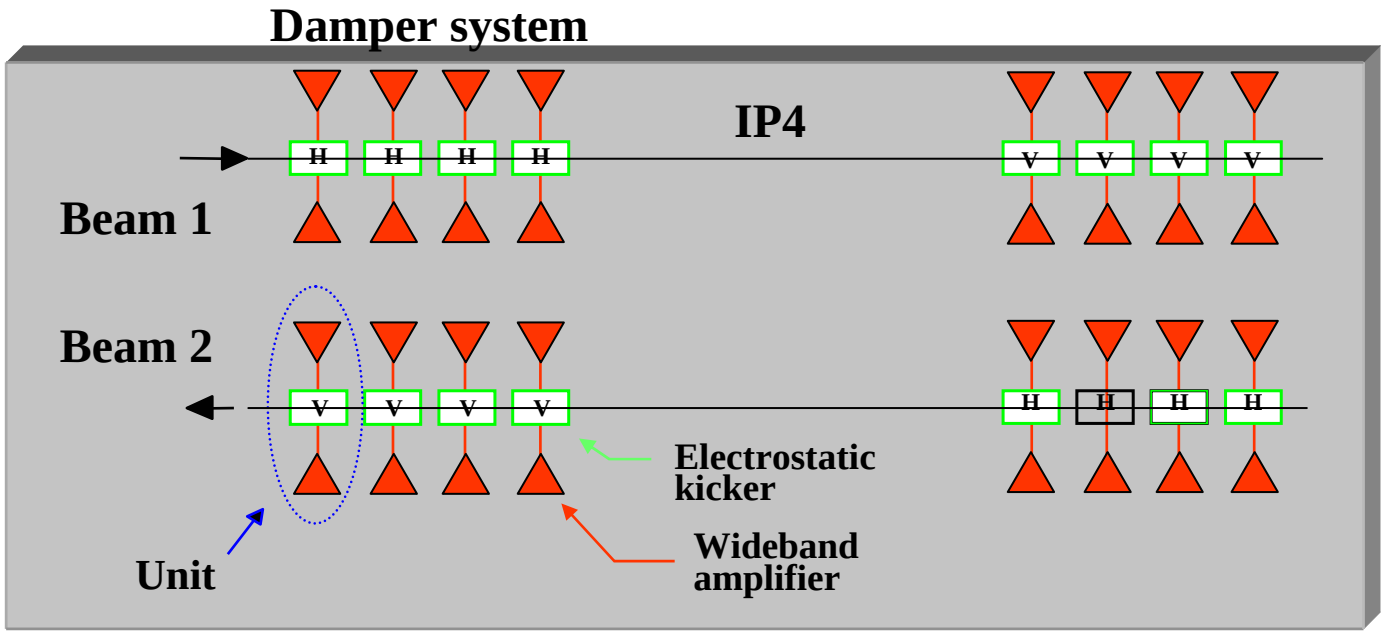
choice:	electrostatic kickers ("base-band")
aperture	52 mm
kickers per beam and plane	4
length per kicker	1.5 m
nominal voltage up to 1 MHz at β=100m	+/- 7.5 kV
kick per turn at 450 GeV/c	2 μrad
rise-time 10-90%, ΔV= +/- 7.5 kV	350 ns
rise-time 1-99%, ΔV= +/- 7.5 kV	720 ns
must provide sufficient gain from	1 kHz to 20 MHz

noise must be less than quantization noise due to 10 bit / 2σ



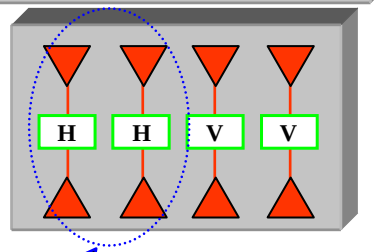
rise time fast enough for gap of 38 missing bunches

The LHC Transverse Damping System (high power part)



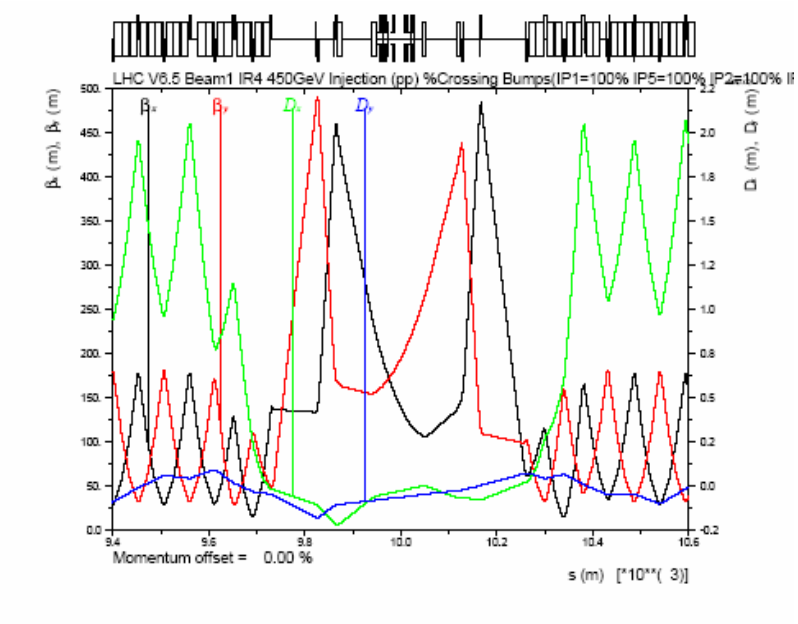
- 20 electrostatic kickers
- 40 wideband amplifiers, i.e. 40 tetrodes (RS2048 CJC, 30 kW)
  20 amplifier cases

+ Spare units

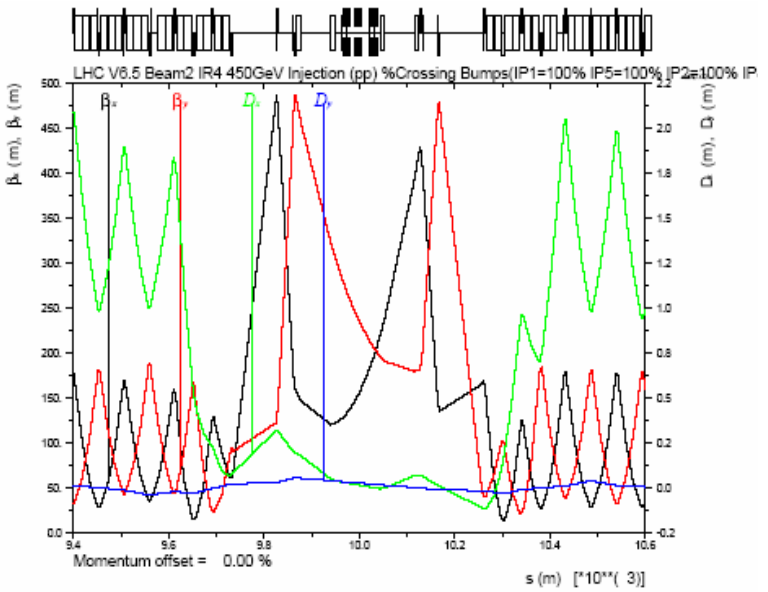


LHC optics at injection in IR4 (beams do not cross!)

Beam 1
high horizontal beta *left* of IP4
high vertical beta *right* of IP4



Beam 2
high horizontal beta *right* of IP4
high vertical beta *left* of IP4



Maximum achievable performance

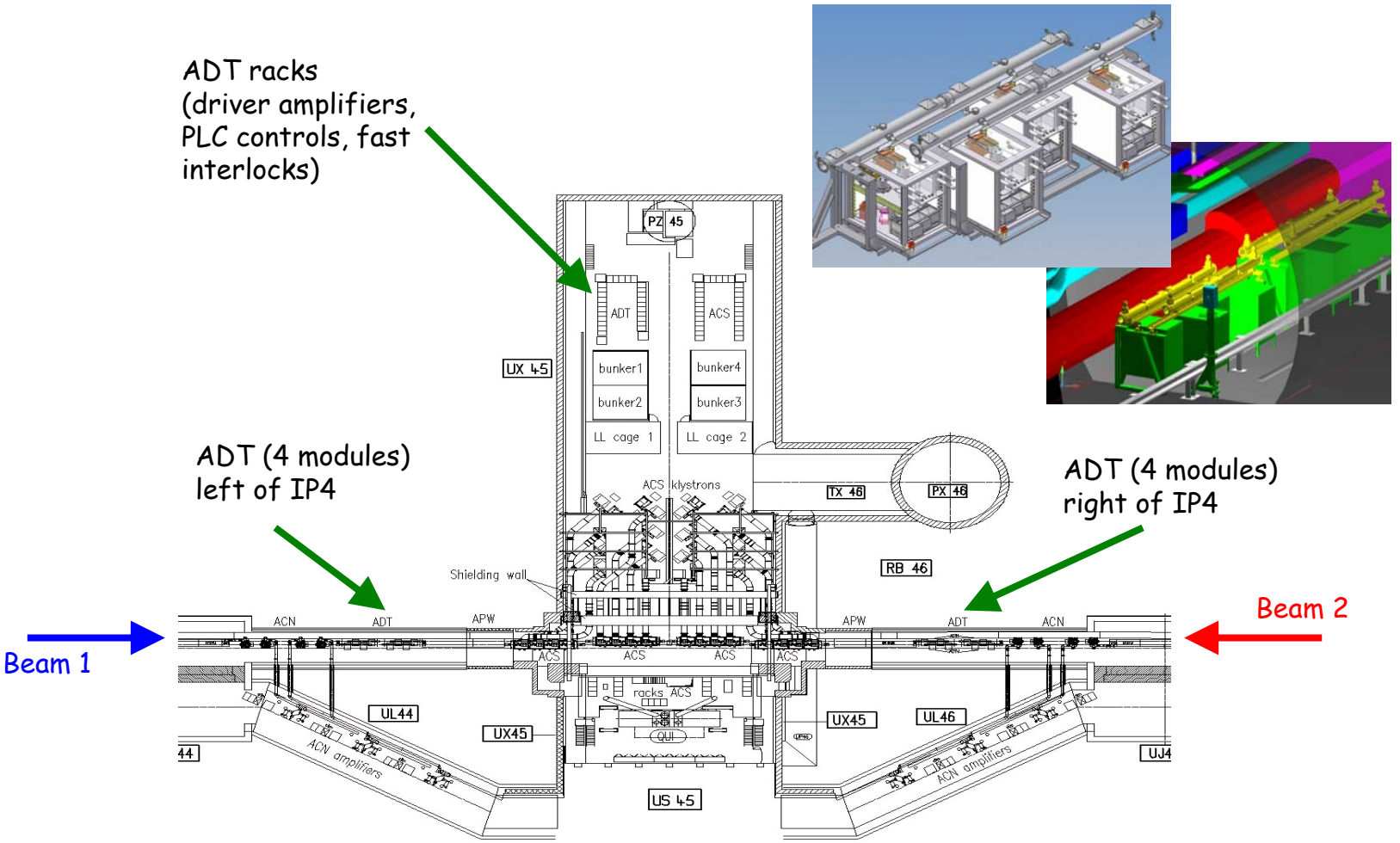
LHCADT performance in LHC optics version 6.4 compared to original assumptions (at **450 GeV/c**), assuming 7.5 kV maximum kick voltage

	β=100 m performance	Optics 6.4 performance
	Kick per turn in σ	Kick per turn in σ @ β in m
ADTH beam 1	0.2 σ	0.277 σ at β=193 m
ADTH beam 2	0.2 σ	0.273 σ at β=187 m
ADTV beam 1	0.2 σ	0.309 σ at β=239 m
ADTV beam 2	0.2 σ	0.316 σ at β=250 m

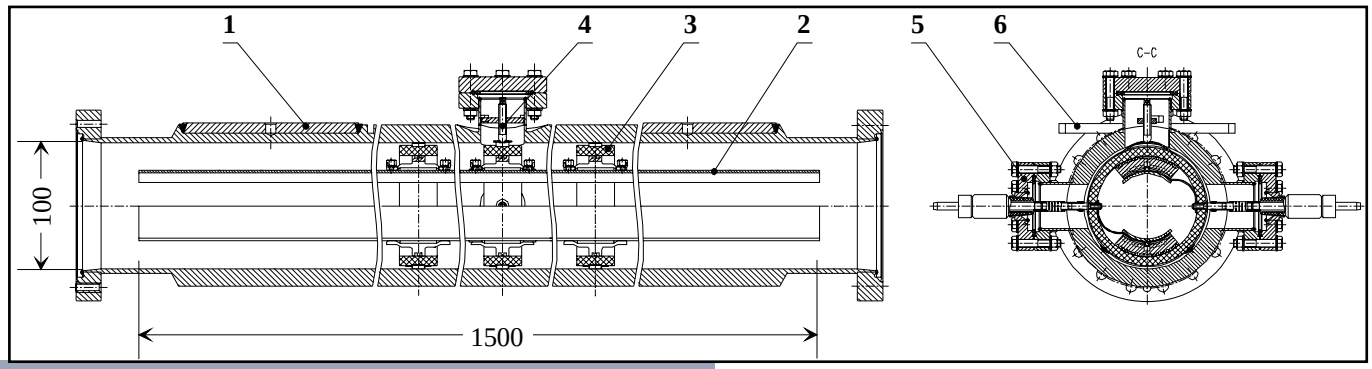
Estimate of maximum capabilities (usage as beam exciter, abort gap cleaning etc.), assumes optics 6.4 as in table above, **450 GeV/c** and running with ~15 kV DC for tetrode anode voltage

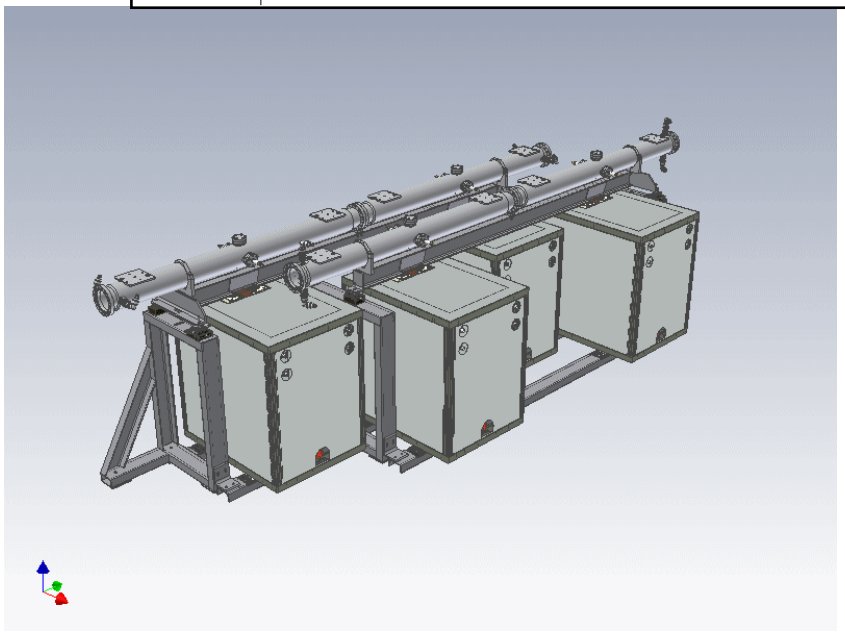
	100 kHz	1 MHz	10 MHz	20 MHz
ADTH	0.47 σ	0.43 σ	0.14 σ	0.05 σ
ADTV	0.47 σ	0.43 σ	0.14 σ	0.05 σ

Physical layout in point 4 underground LHC



Kicker design





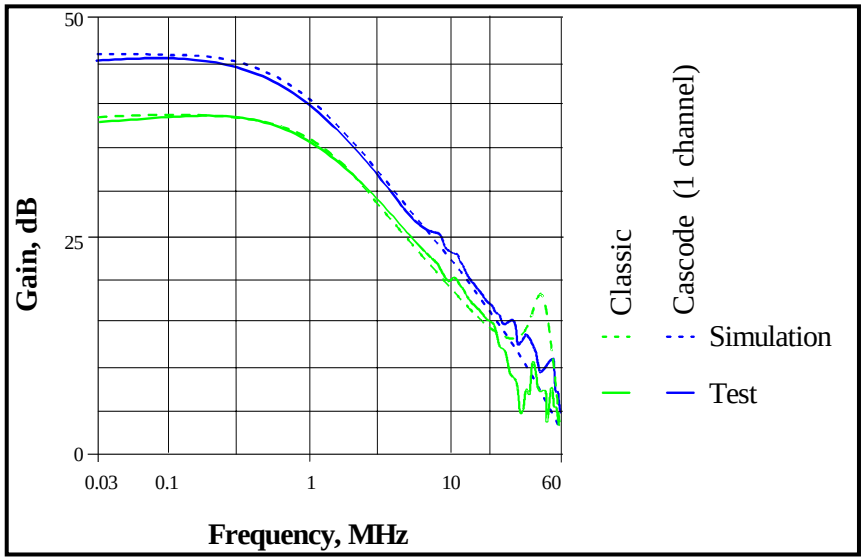
- Prototype kicker delivered and tested with power amplifier at CERN; series production has started in Russia
- Vacuum testing planned at CERN for November 2005; installation in LHC tunnel in February 2006, vacuum interconnection in March 2006, progress depends on advance with cryoline in LSS4

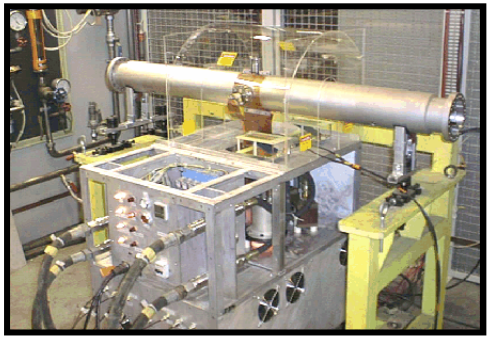
Testing of power amplifier

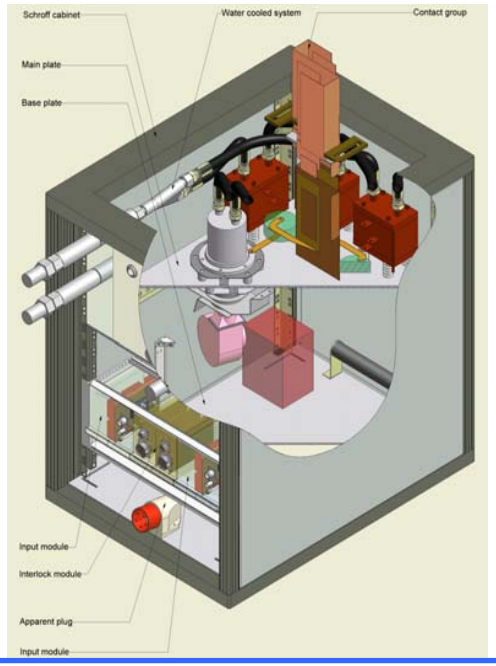
Prototype manufactured
and tested in 2001; +/- 10 kV achieved, 1 kΩ load in amplifier

Production series design
and manufacturing 2002-2006

Nonlinear phase vs frequency
will be compensated in low-level
(kicker is a capacitive shunt at high frequencies)



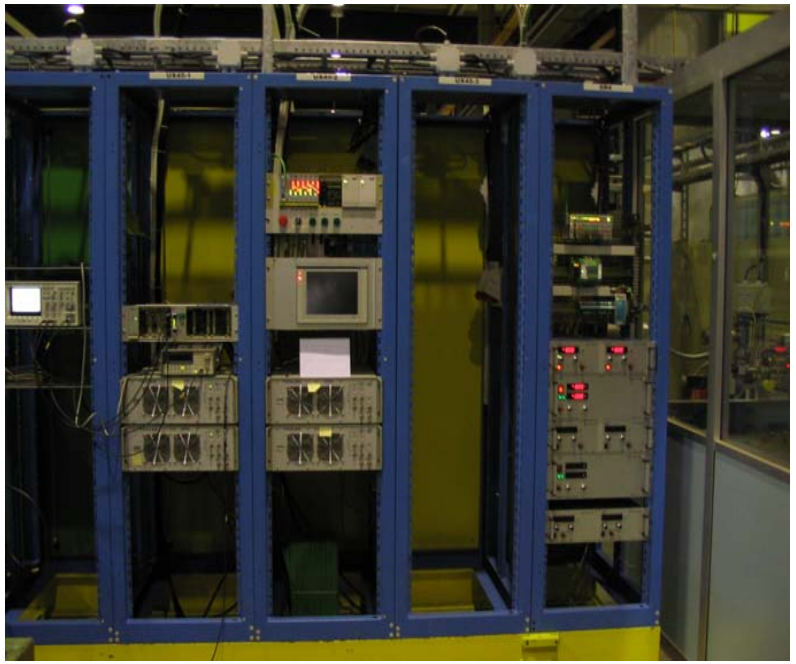




Power amplifier and test stand at CERN operational since July 2005

Two power amplifiers and their kickers

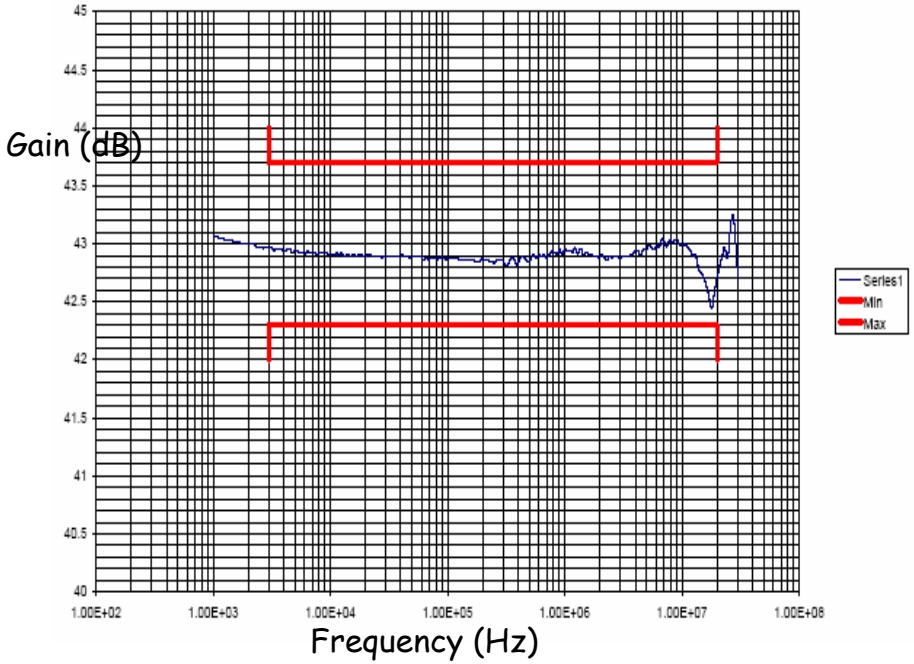
Control racks with 200 W driver amplifiers and PLC controls with interlocks



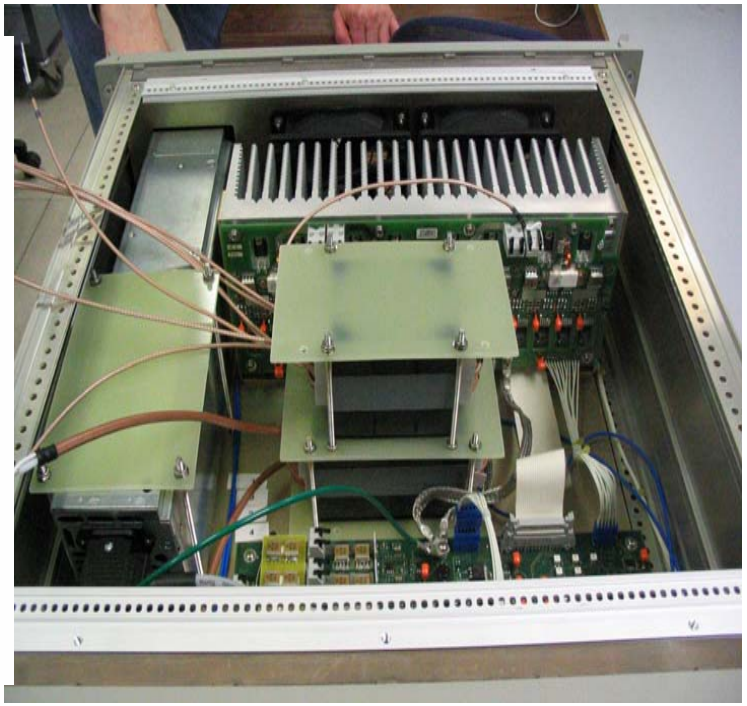
200 W solid state driver amplifier (1)

Experience from the SPS damper with in-house developed driver amplifiers showed that the driver amplifier is one of the most critical items with respect to performance and reliability

43 dB gain, very flat 3 kHz – 20 MHz



For the LHC damper industry developed a custom design amplifier inspired by the design of the SPS amplifiers;
40 amplifiers have been manufactured and tested

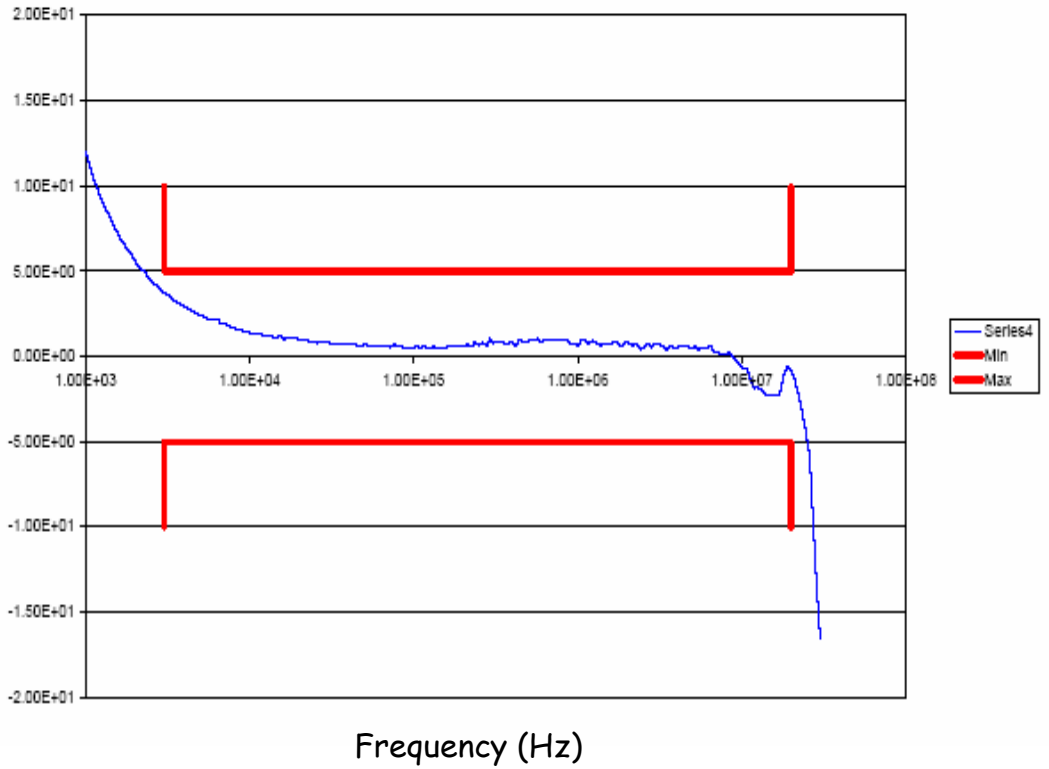


200 W solid state driver amplifier (2)

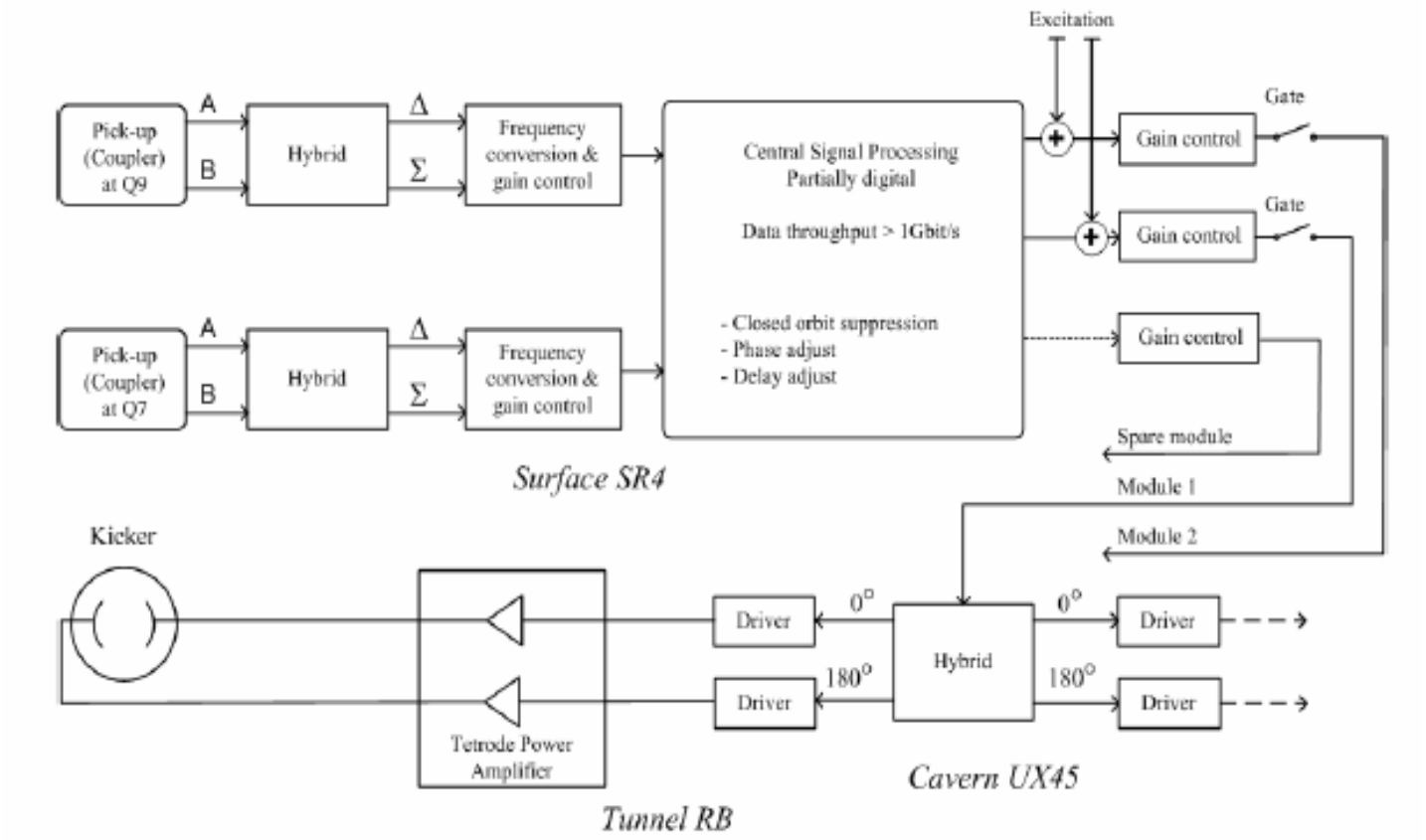
200 W output power max CW

3 kHz to 20 MHz at up to 100 W achieved:
< +/- 0.5 dB gain ripple
+/- 5 degree phase variation from linear phase
constant group delay < +/- 0.1 ns (also from amplifier to amplifier)
< -30 dBc 3rd harmonic distortion

Fulfills spec for interference and noise (10 mV rms and spikes limited to 50 mV peak)



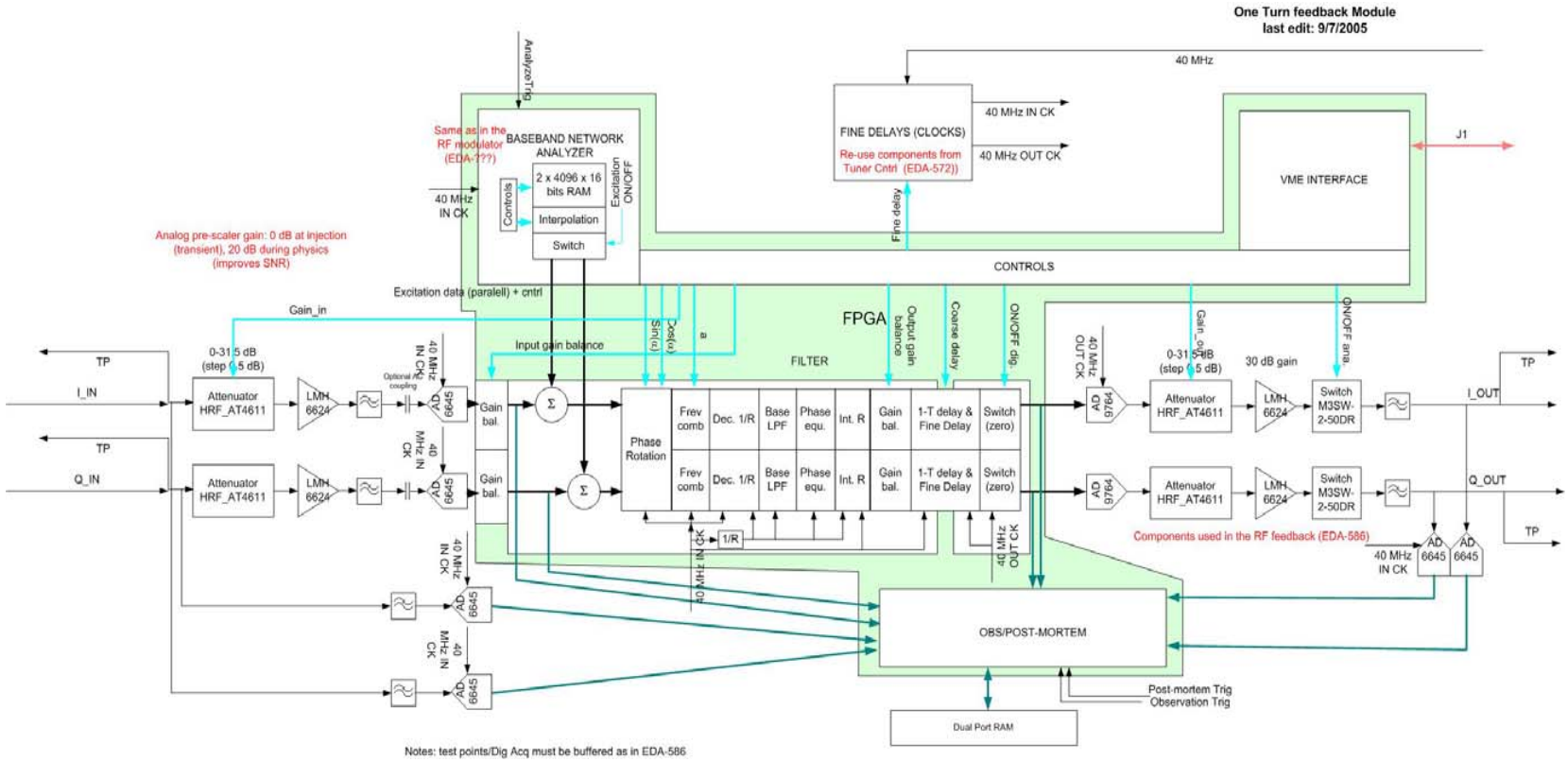
Overview of one Damper system



LHC ADT Low level electronics

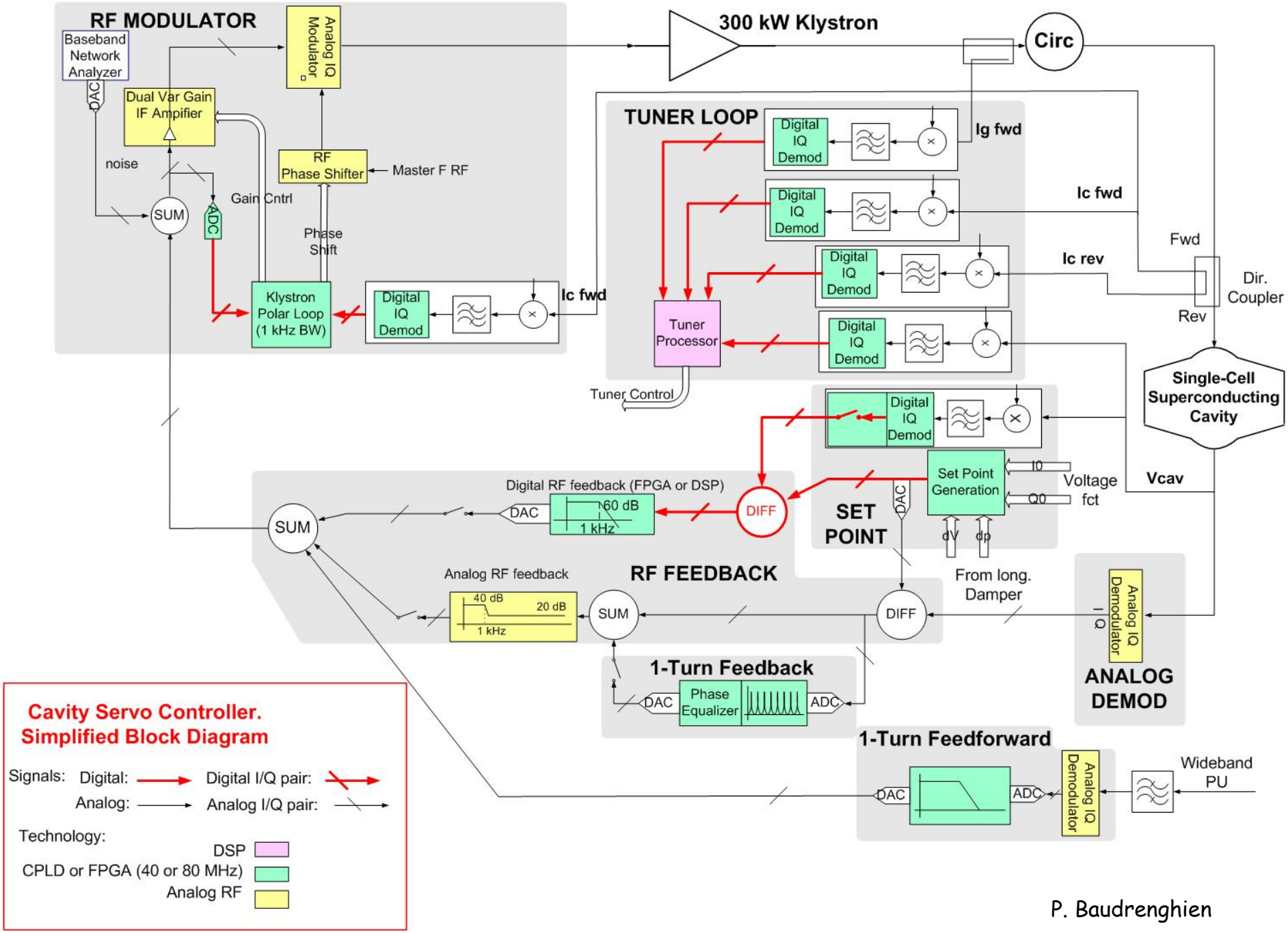
- System will be based on experience gained with SPS Damper
- Two coupler type pick-ups with betatron phase advance of ~90 degrees will be installed (BDI group)
- Spectrum repeats every 40 MHz (25 ns bunch spacing) -> analogue down mixing with a multiple of 40 MHz to baseband , LO probably 320 MHz
- One of the horizontal pick-ups is installed at zero dispersion and it will be possible to use this pick-up and a Hilbert transformer (FIR filter) for the phase adjustment if wanted; Hilbert filter tested in SPS but not used in operation (reduced phase stability margin at very high gain)
- FPGA technology for implementing most of the functions digitally (notch filter, fine delay adjustment, betatron phase adjustment by two pick-ups or Hilbert filter and single pick-up use)

Synergy between LHC- 1-Turn longitudinal feedback and transverse damper - use same hardware



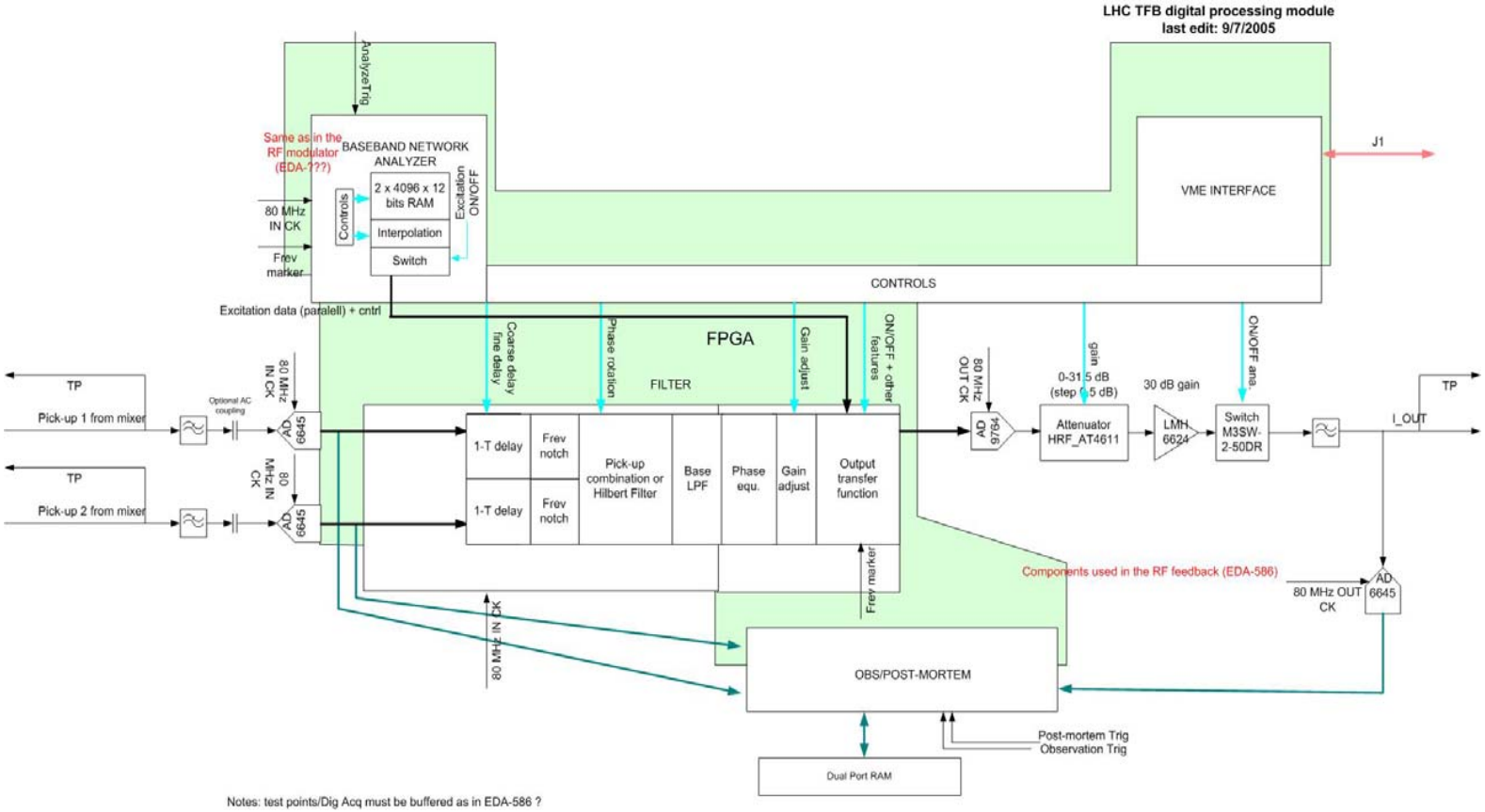
FPGA code done (V. Rossi); board layout under way

P. Baudrenghien



P. Baudrenghien

LHC Damper signal processing coarse layout



planned to launch FPGA coding early 2006, further synergy with PS transverse damper project and later lonitudinal PS 1-T cavity feedback (2008)

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