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Multi bunch instabilities and cures at the SLS

M. Dehler, P. Pollet, R. Kramert, G. Marinkovic, T. Schilcher (PSI)
D. Bulfone, M. Lonza (ELETTRA)

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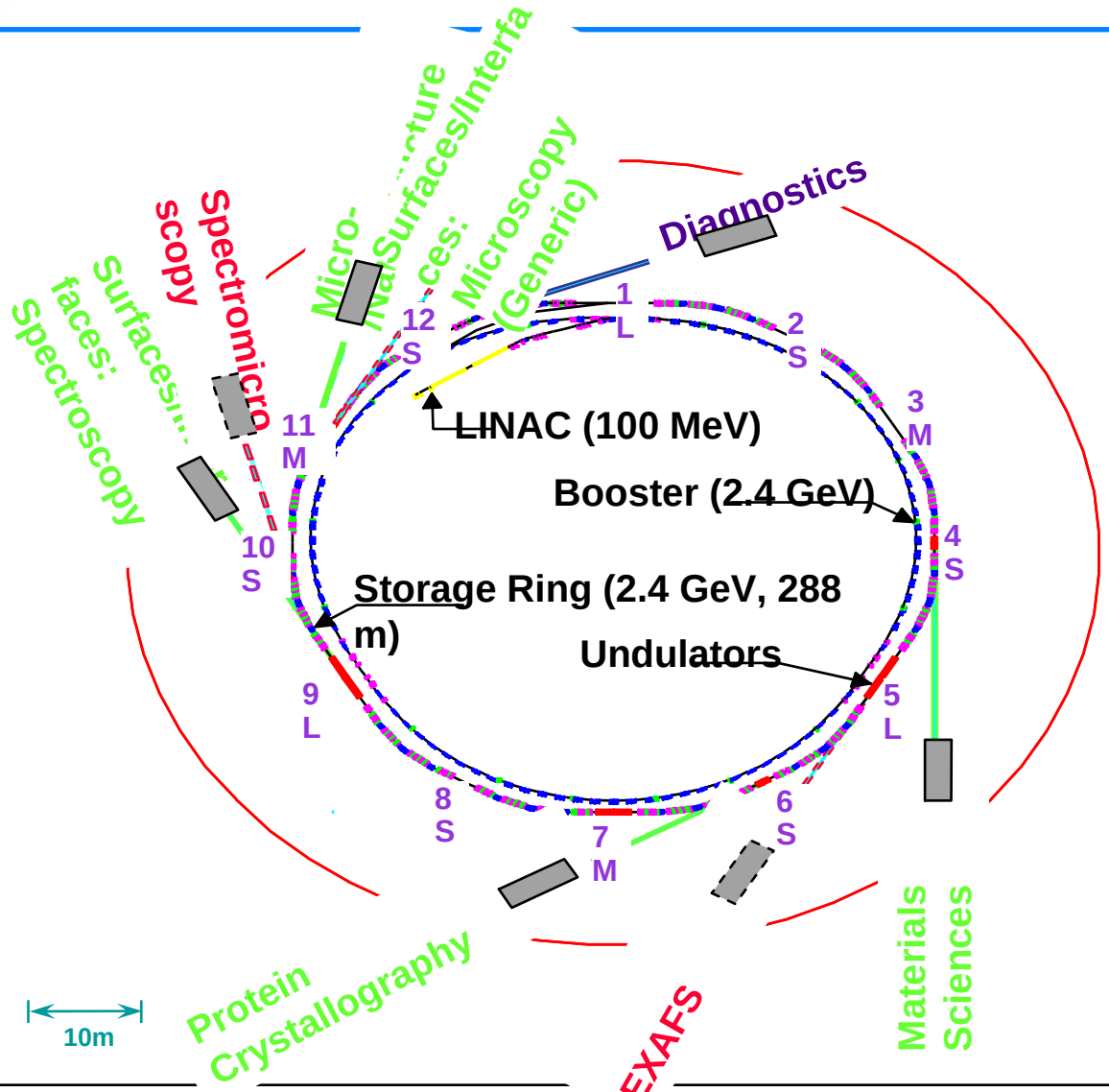
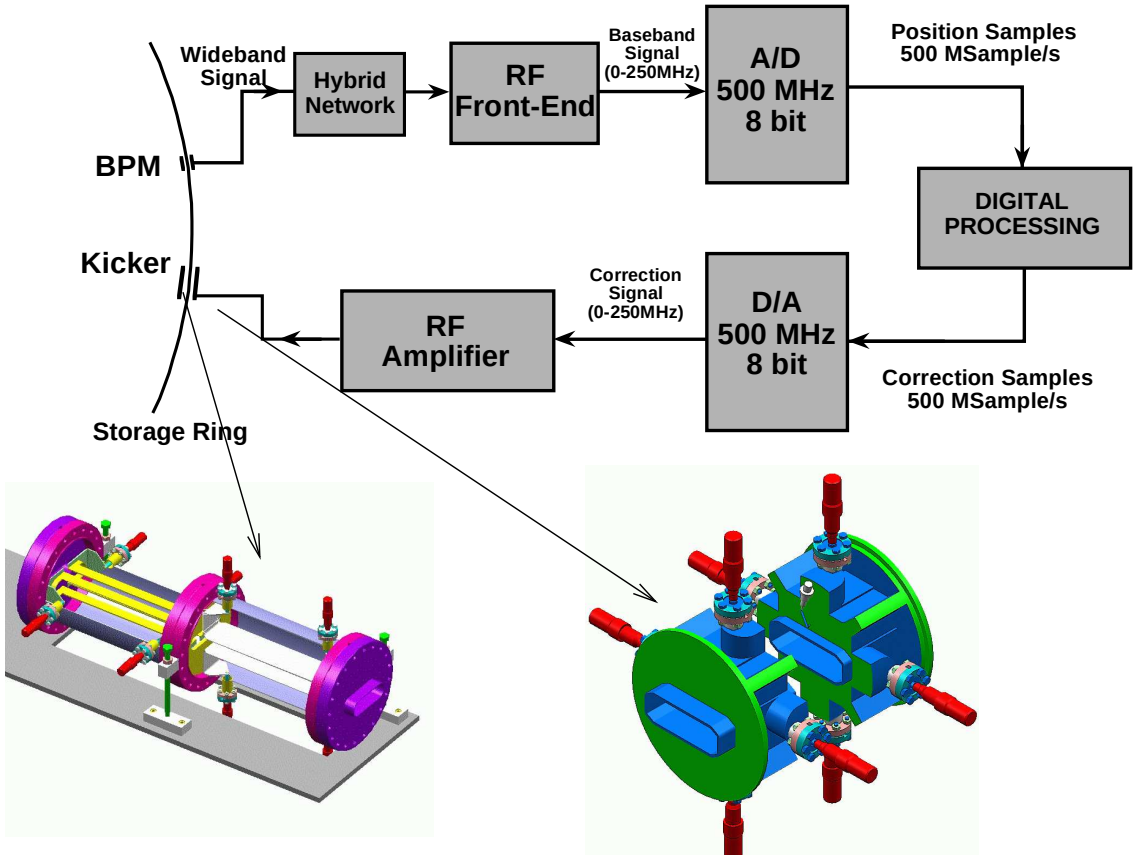
Aerial view of PSI

SLS - BEAMLINES



The lines marked in green indicate the planned beamlines of the first generation from "insertion devices" like wigglers, wavelength shifters or undulators and from superconducting bending magnets. The lines marked in red indicate second phase beamlines.

(Historical) Overview



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Theoretical performance

Feedback Parameters		
General:	Vert.	Hor.
Tune ν	7.08	20.82
Damping time τ_{nat}	9.0 ms	9.0 ms
Driving Impedances (max)		
Resistive Wall	0.9 MΩ/m	0.06 MΩ/m
Cavity HOM	45 MΩ/m	45 MΩ/m
Filter type	2-tap	2-tap
Eff. damping time	$9\mu s$	$48\mu s$
Max. stable impedance	$105M\Omega/m$	$107M\Omega/m$
Kicker parameters:		
Strength $R_s = V_{\|\|}^2/2P$	$20.0K\Omega$	$14.5K\Omega$
Kick ($\delta\hat{x} = 55\mu m$)	$2800V$	$2400V$
Input power per port ($\delta\hat{x} = 55\mu m$)	$200W$	$200W$
Capture Limit for spec. max. power (Only resistive wall)	$6.4mm$	$94mm$
Noise sensistivity:		
Noise source: RF FE/ADC $\delta x_{rms}(generated)/\delta x_{rms}(measured)$	0.2	0.07
Noise source: DAC/PA (-40 dB Noise assumed.)	$0.15\mu m$	$0.07\mu m$

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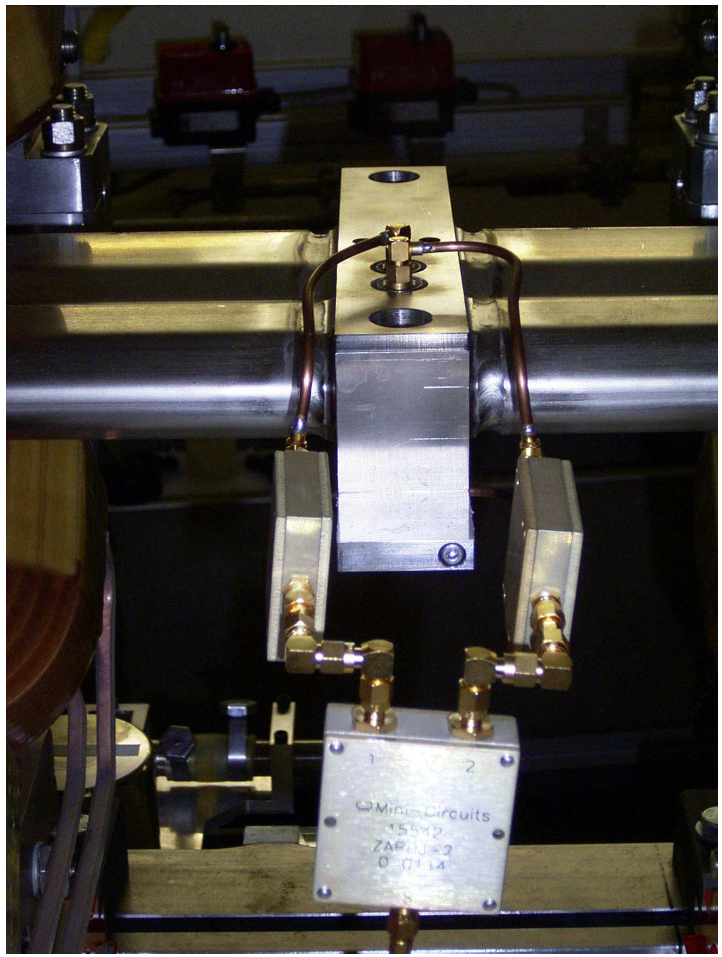
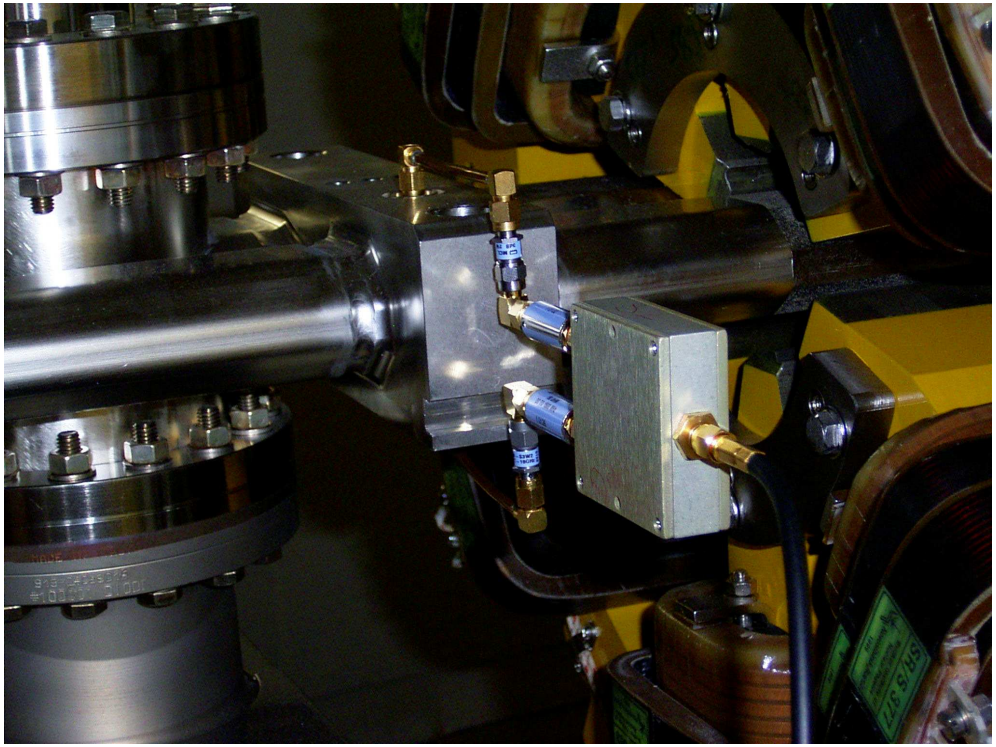
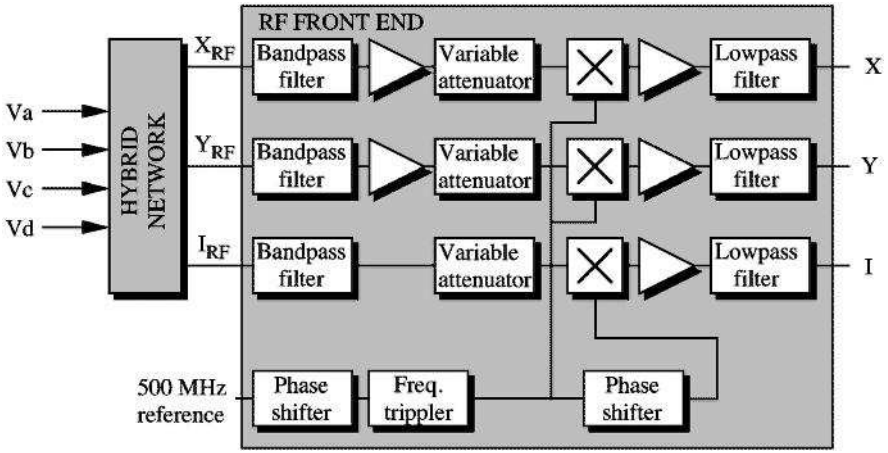
H/V pickups with hybrids





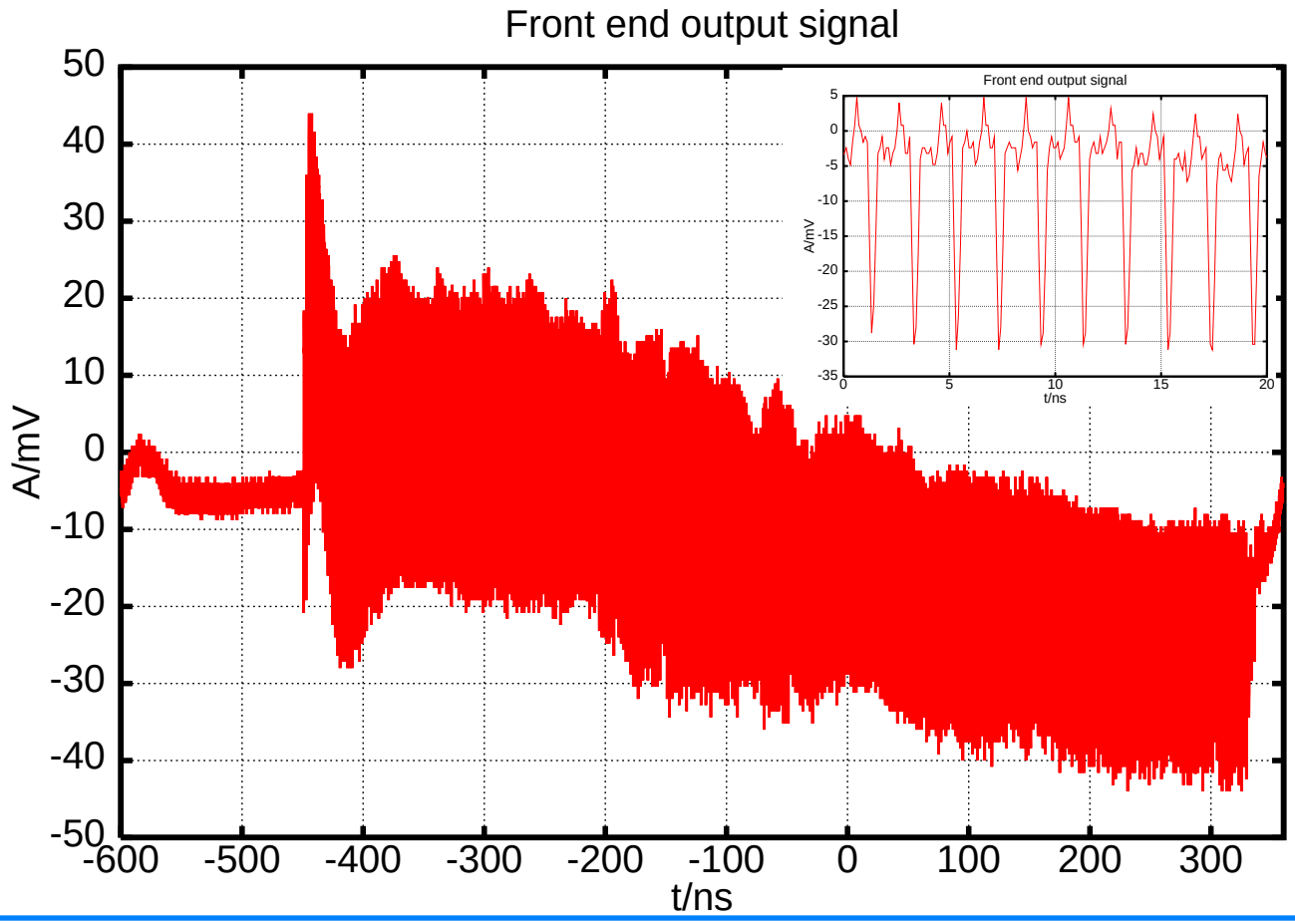
RF front end



Parameter	Specification
Center frequency	1.5 GHz
X,Y input signal range	-49 dBm to -29 dBm
I input signal range	-23 dBm to -3 dBm
X,Y channel noise figure	5 dB at -49 dBm input
Output spectrum window	40 kHz to 250 MHz
Max output level	1 Vp-p or +4 dBm at 50 ohm
Overall bandwidth	
1 dB	250 MHz
3 dB	300 MHz
20 dB	400 MHz
Phase shift control range	> 430 degrees at 1.5 GHz
Gain control range	20 dB

Beam response

Typical signal trace



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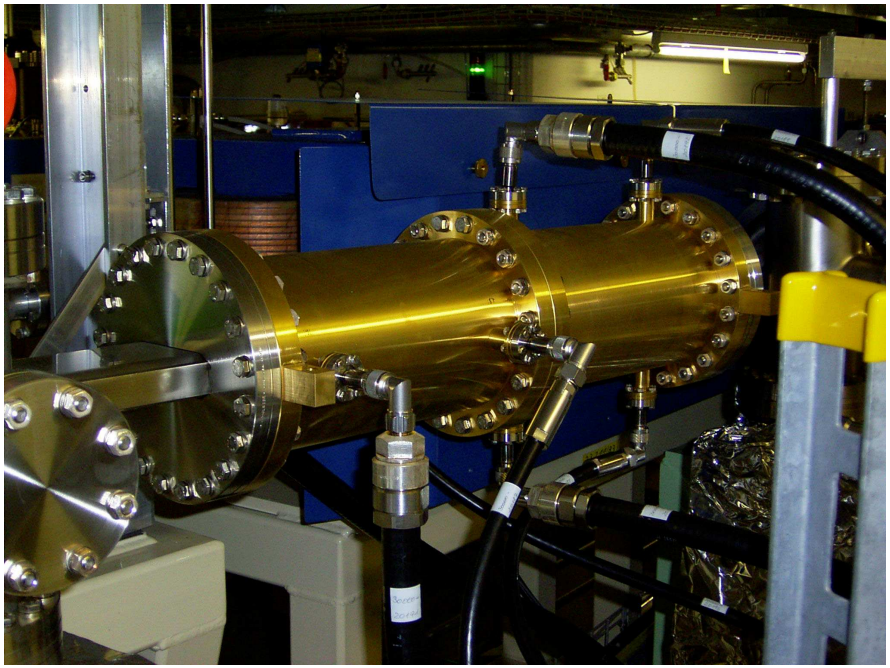
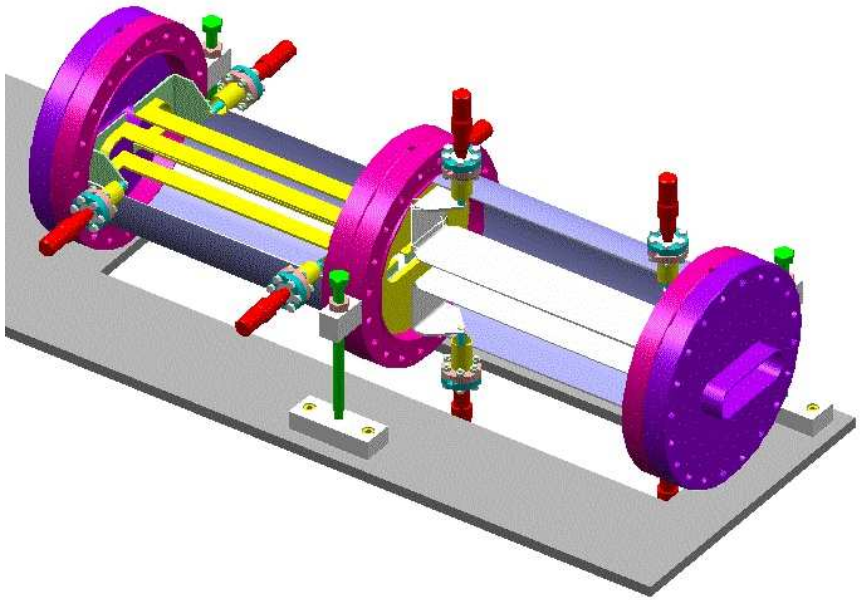
Transverse kickers





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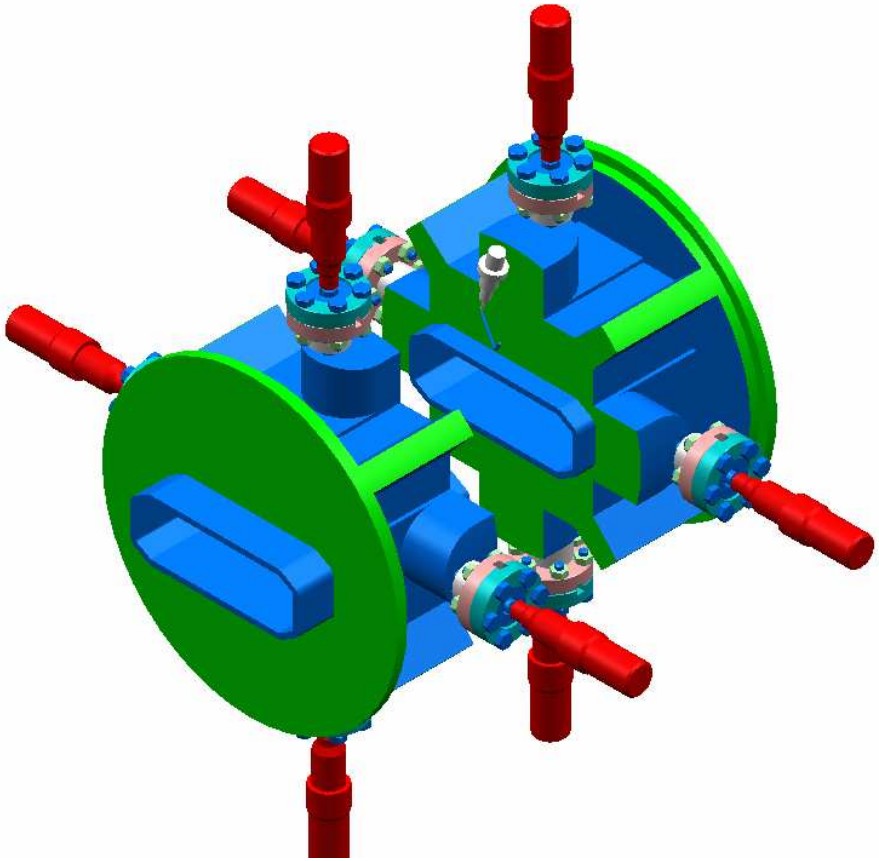
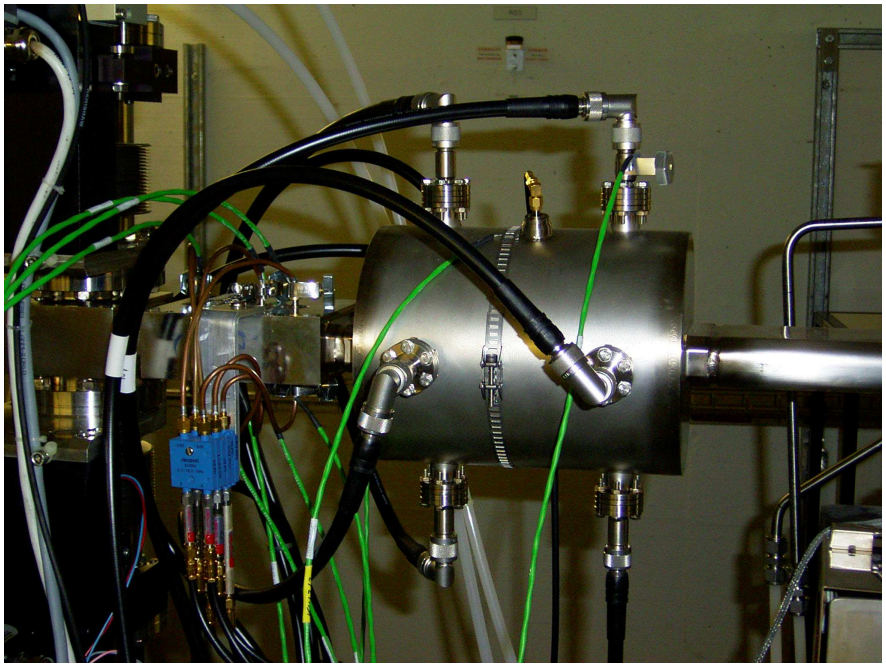
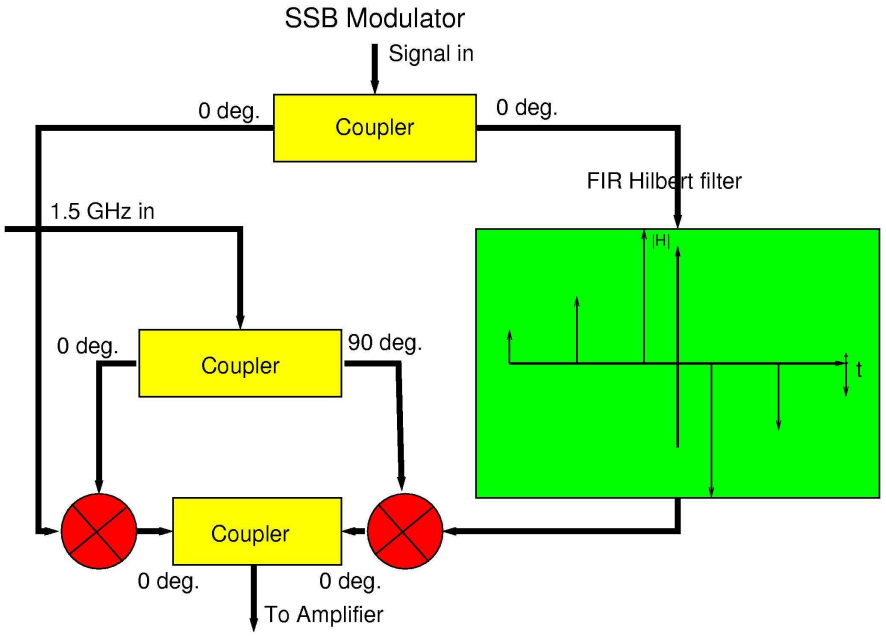
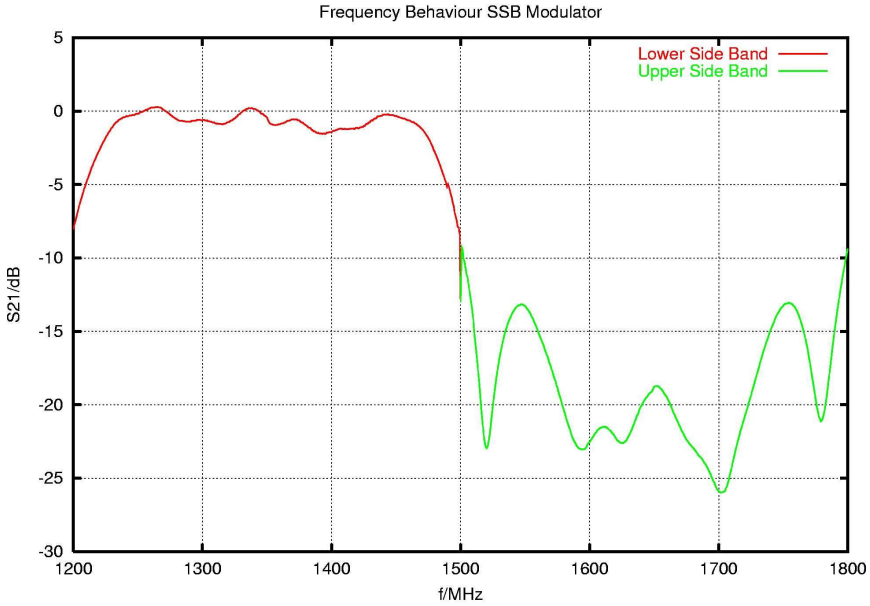
Longitudinal kicker

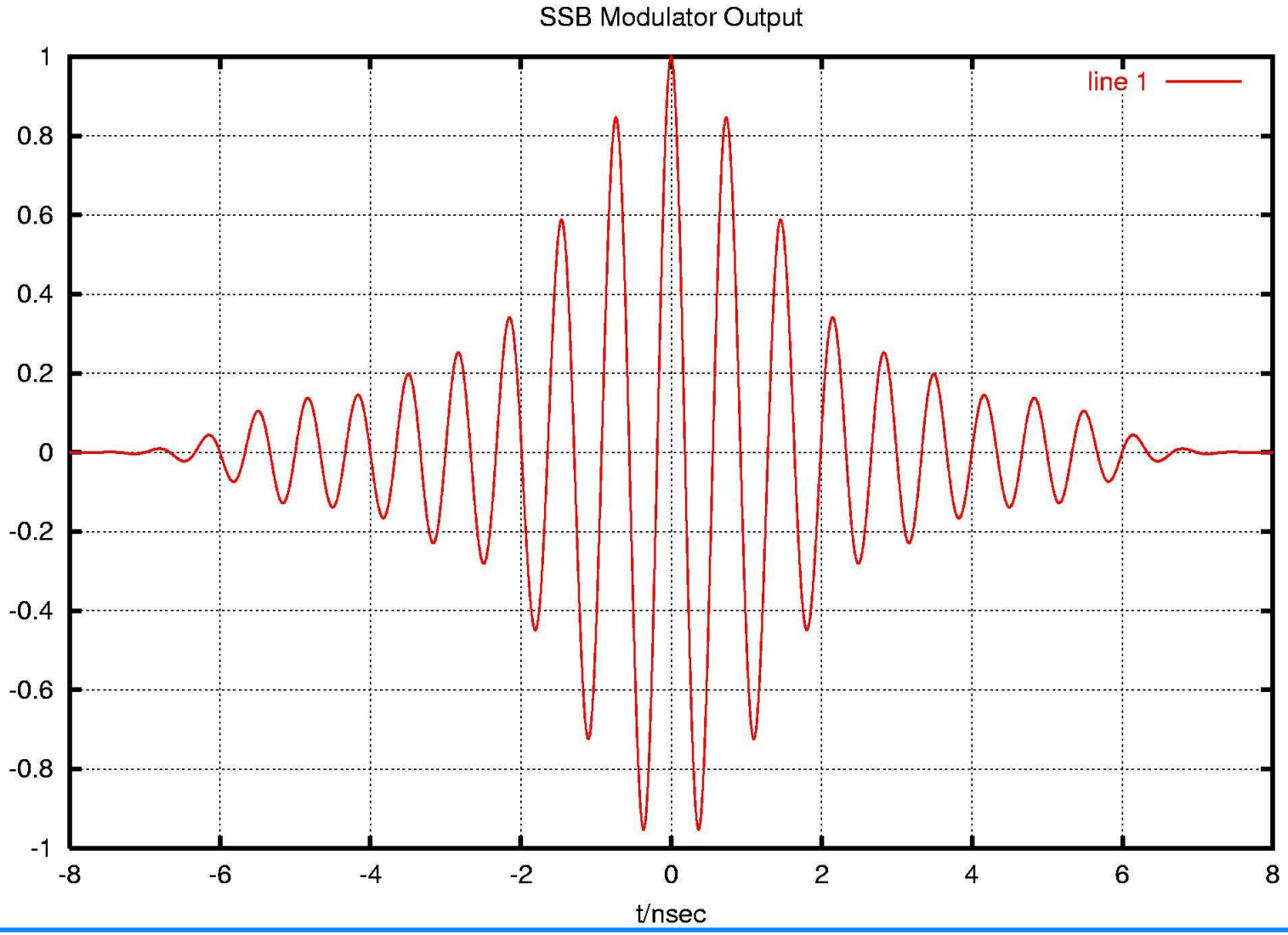




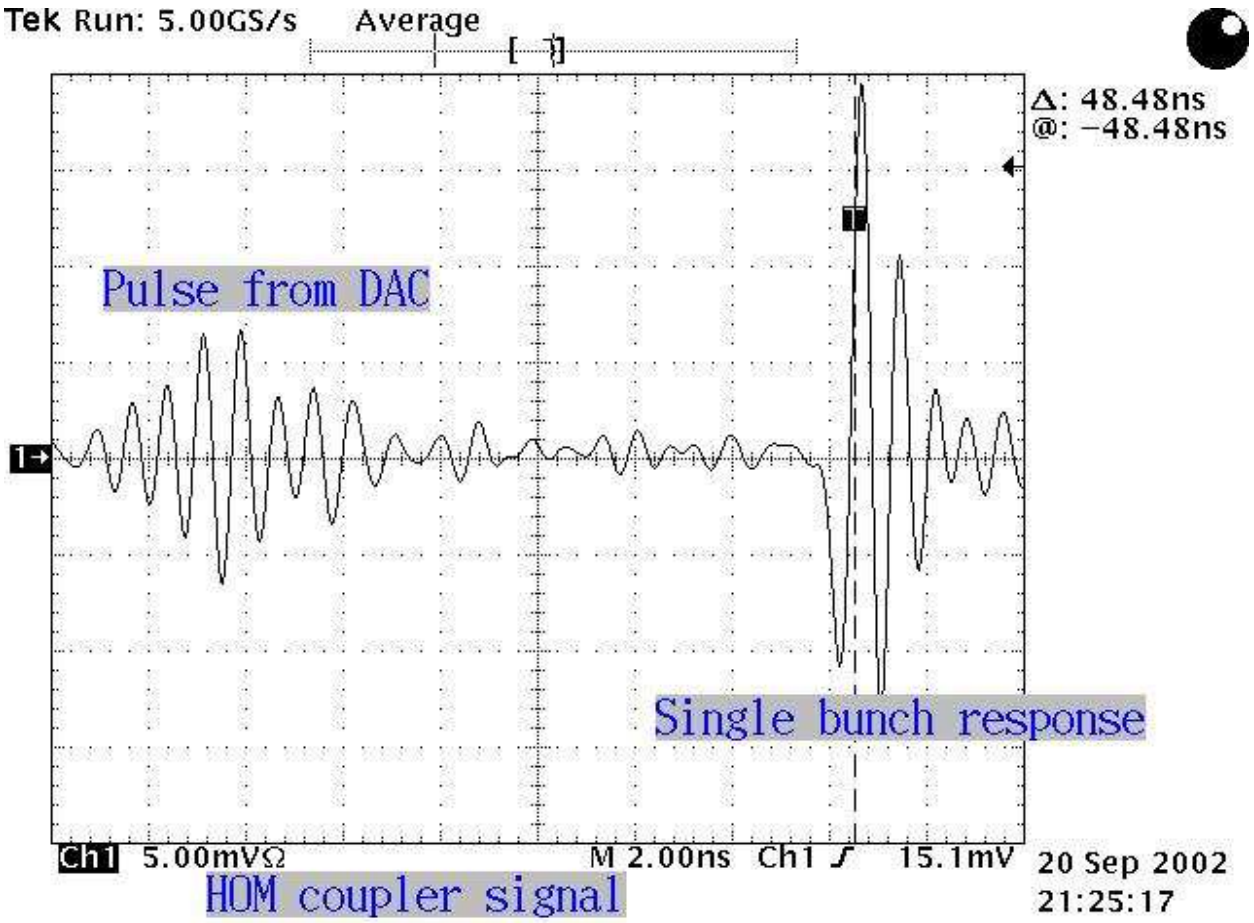
SSB modulator for longitudinal plane (Others use QPSK?)

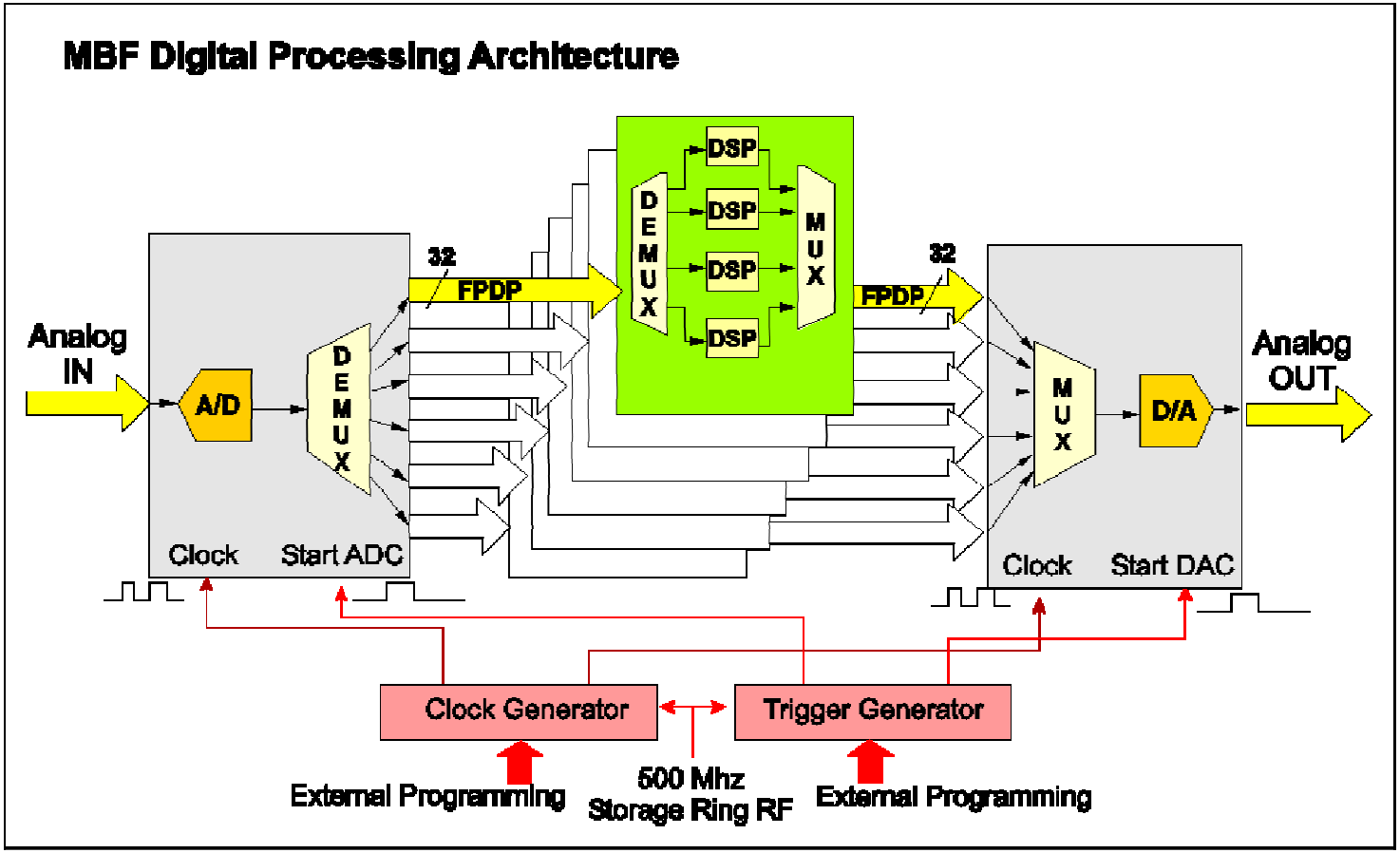




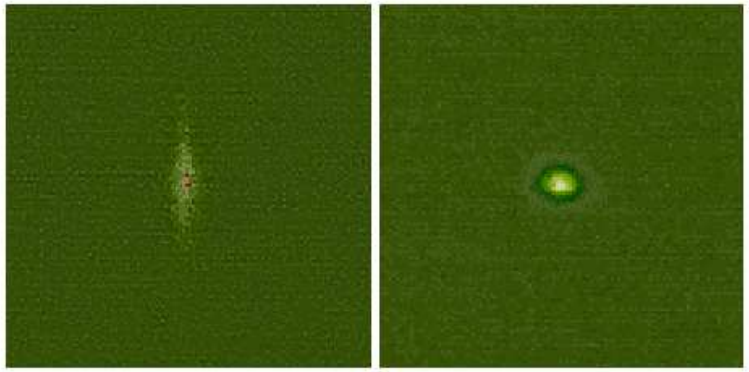

SSB Modulator Output
line 1
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-8
-6
-4
-2
0
2
4
6
8
t/nsec

Pulse response: SSB + Filter + Kicker

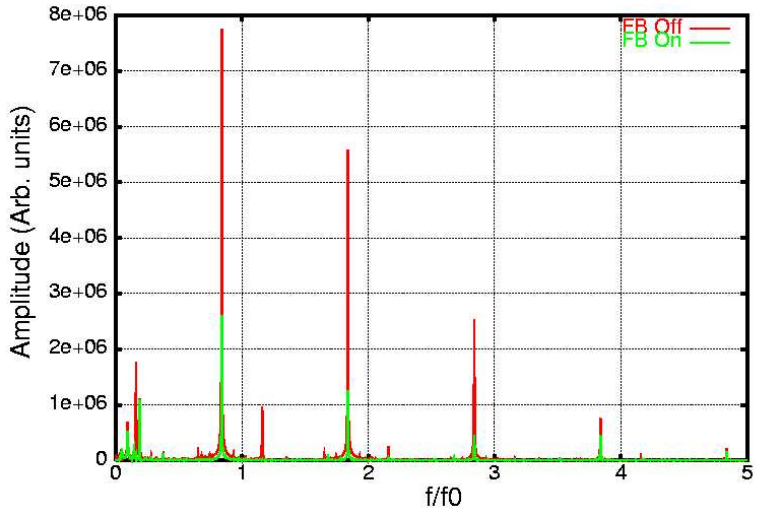



MBF Digital Processing Architecture
Analog IN
A/D
DEMUX
32
FPDP
DEMUX
DSP
DSP
DSP
DSP
MUX
32
FPDP
MUX
D/A
Analog OUT
Clock
Start ADC
Clock
Start DAC
Clock Generator
Trigger Generator
External Programming
500 Mhz Storage Ring RF
External Programming

Boring, but true:
Early performance of bunch by bunch feedback



MBF off **MBF on**



BUT

No more

ADC & DAC boards

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Specs for in house ADC/DAC development

Sampling Rate	200-500 MHz
Resolution	8 bits
Input Impedance	50 Ω
Coupling	AC
Analog Bandwidth (3 dB)	5kHz - 500 MHz
In-band Phase Rotation	$< 10^o$
Input Level(ADC)	0 dBm
Output Level(DAC)	6 dBm
Signal/Noise + Distortion Ratio (Total Dynamic Distortion)	> 40dB
External Clock	Sine Wave/DECL
Clock Programmable Shift	Range > 2ns, steps < 100 ps
External Trigger	DECL
Total Jitter from Clock Input to Analog I/O:	< 10 ps
VME interface	VME64x compatible A32/D32 (base address geographic) or switch selectable)
FPDP Interface	ANSI/VITA 17 Single Ended TTL, 80 pin connector
Number of FPDP Ports	1 to 12
Memory Size	8 MByte

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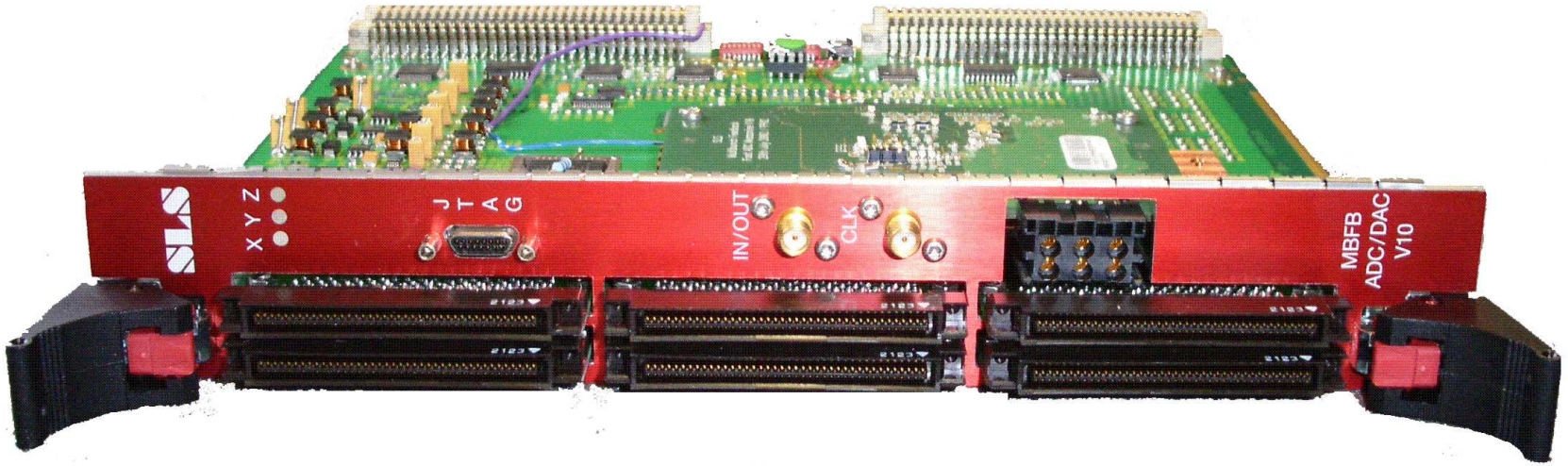
Sandwich structure with three layers:

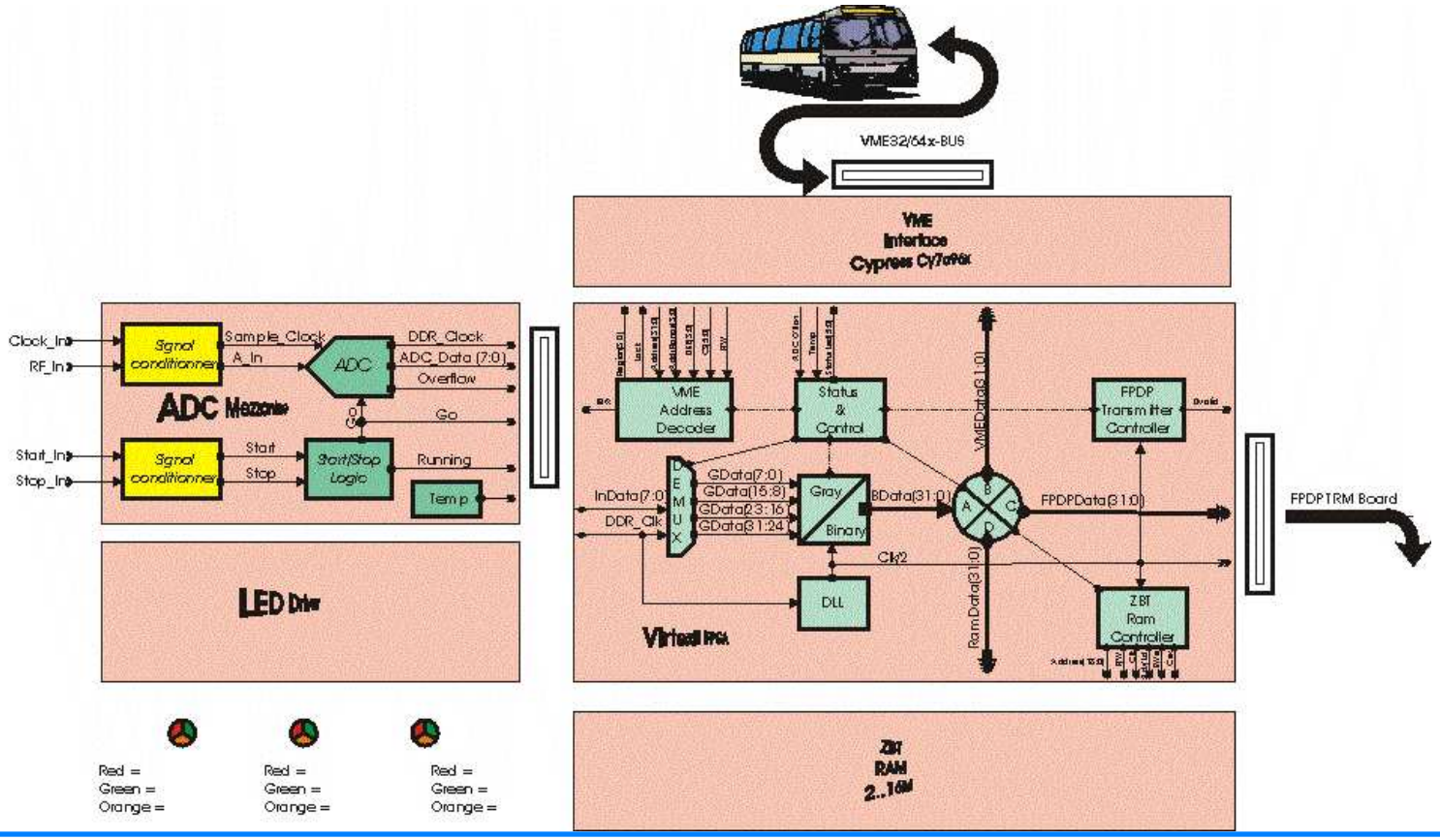
- **Mezzanine boards with ADC or DAC**
- **Main board with VME interface, Virtex FPGA and RAM (common design for ADC and DAC)**
- **FPDP board with second (de−)multiplexer stage (common for ADC and DAC)**

(For multiplexing ratios greater six: fourth board carrying additional FPDP connectors)



Functional blocks

Basic Layout ADC



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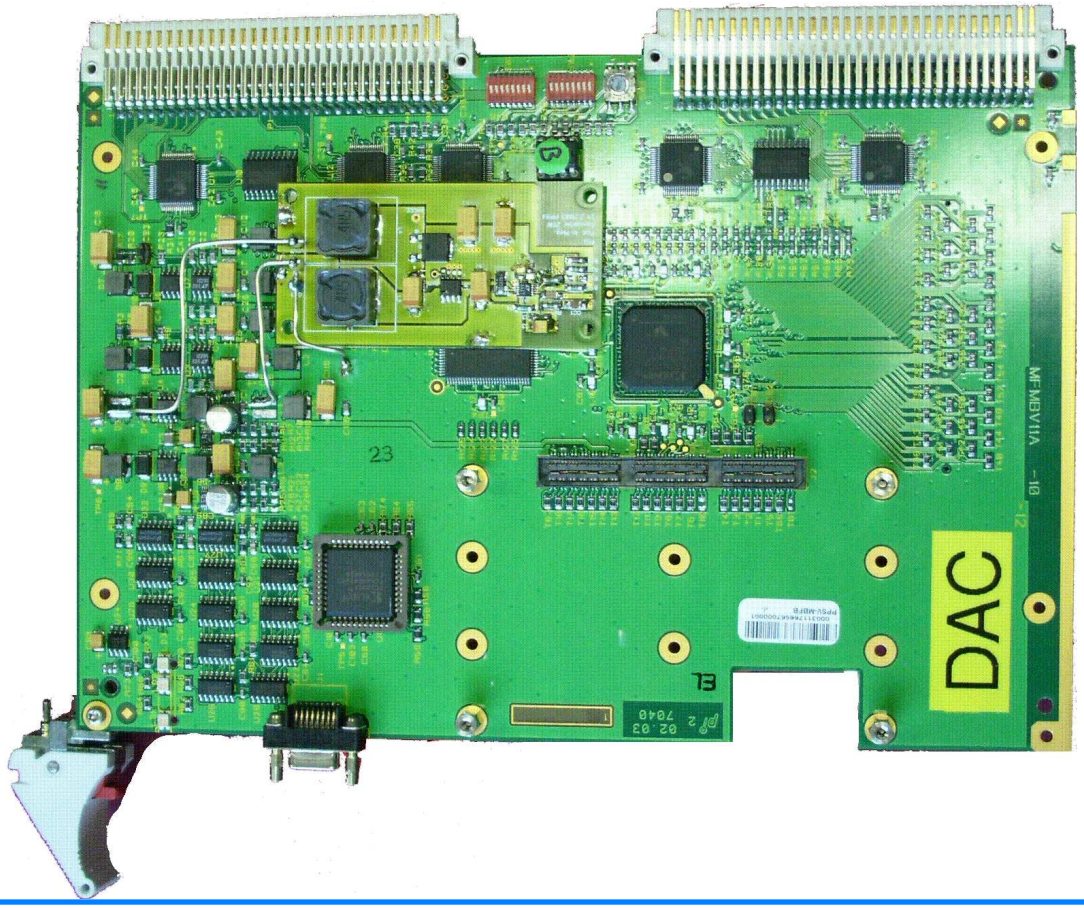
Main board

Main complexity hidden within FPGA firmware



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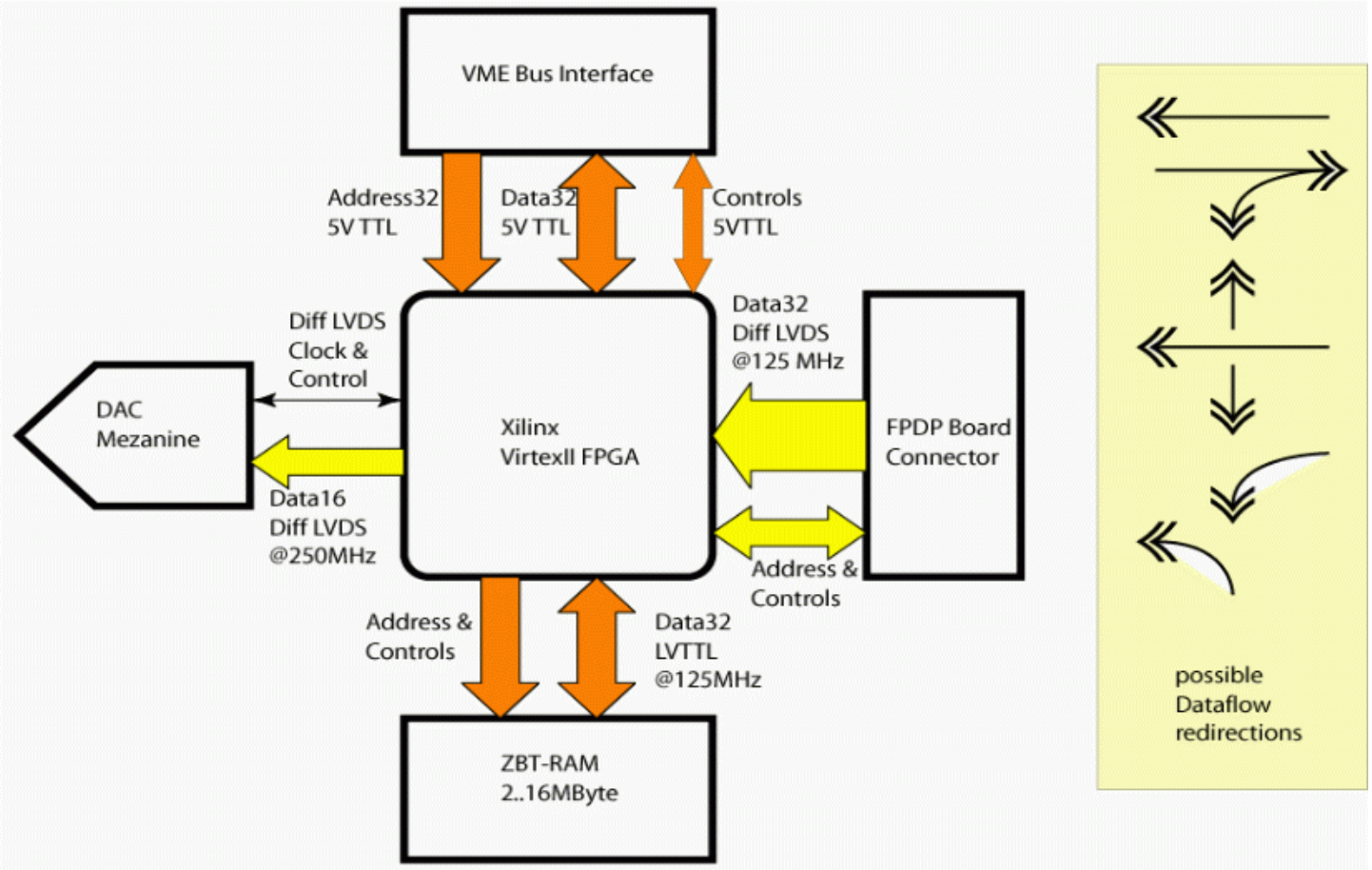
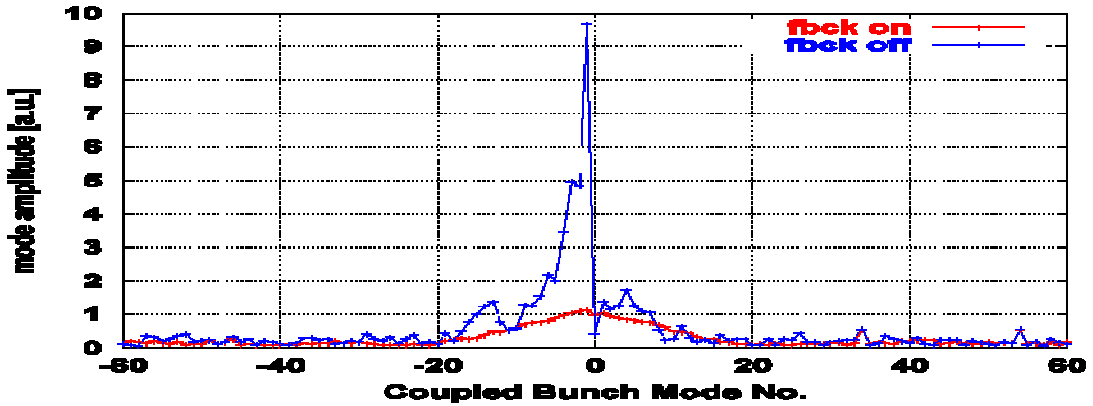
Options for data flux



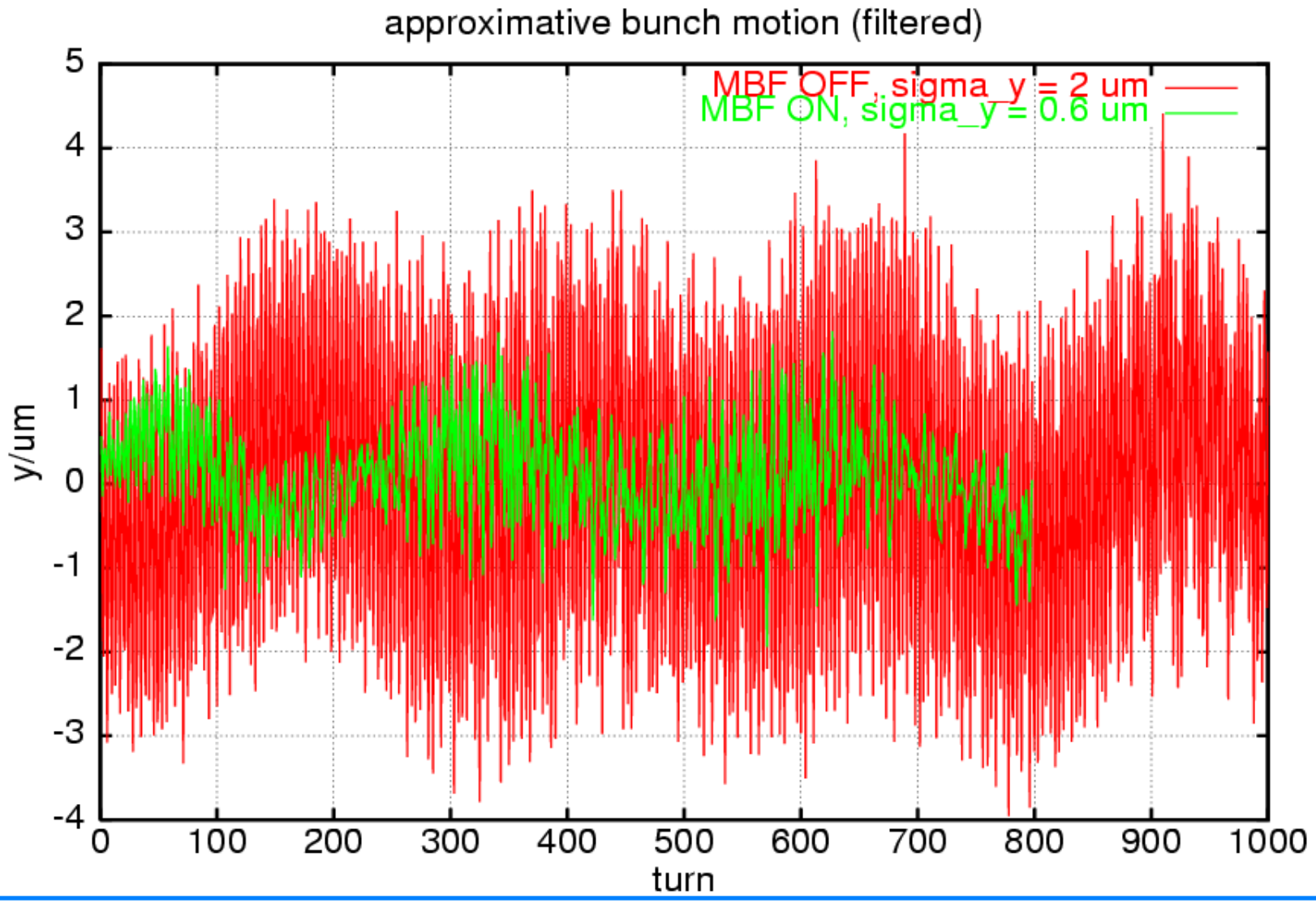
Closed loop



For long time had problems with non reproducible settings for ADC/DAC latency

(hopefully resolved by now)

Transverse system 95% complete


approximative bunch motion (filtered)
MBF OFF, sigma_y = 2 um
MBF ON, sigma_y = 0.6 um
y/um
turn
5
4
3
2
1
0
-1
-2
-3
-4
0
100
200
300
400
500
600
700
800
900
1000

Status from the user perspective

Vertical plane:

Slight instabilities, not visible for users (but they are getting more sophisticated ...)

Horizontal plane:

Stable. FB may help to close bump of injection kickers (Top up!)

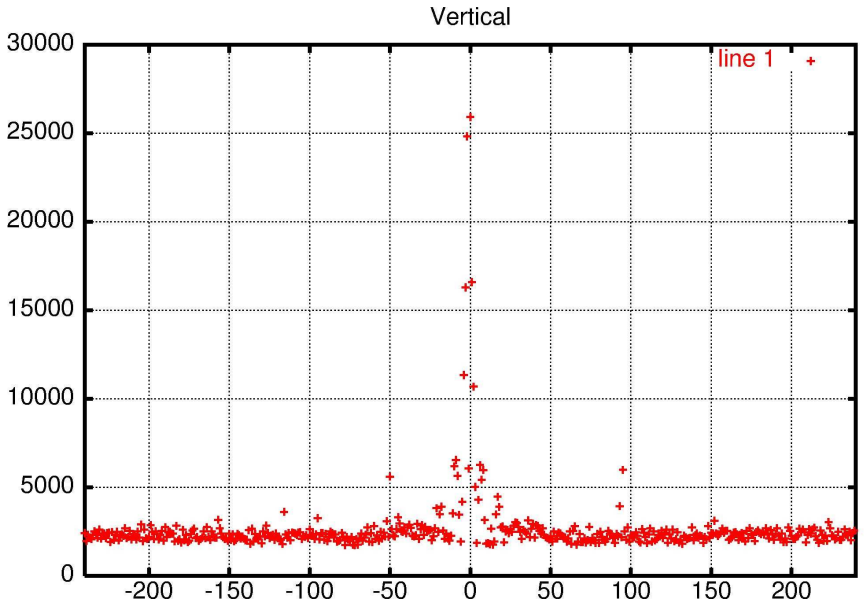
Longitudinal plane:

Stable. Fallback, if 3 HC cavity gets in normal conducting state (Otherwise Ibeam <180 mA).

General:

More freedom in settings (Chromaticity)

Fill pattern feedback?



Typical CBM spectrum during user operation